EE 505

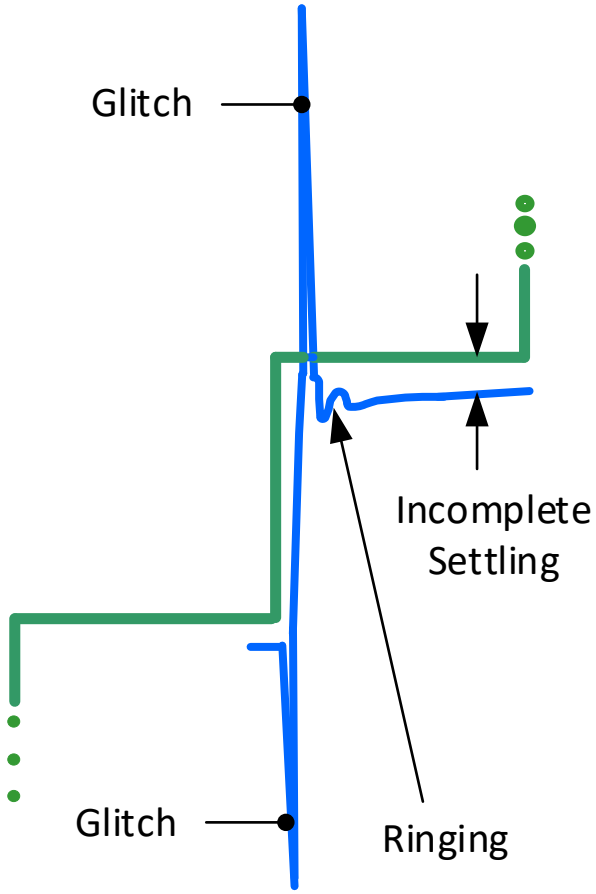
Lecture 14

String DACs

Current Steering DACs

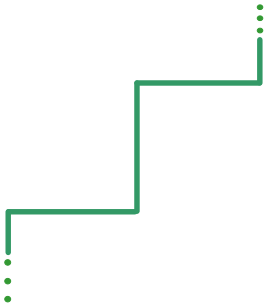
Review from Last Lecture

DAC Performance Issues and Concerns

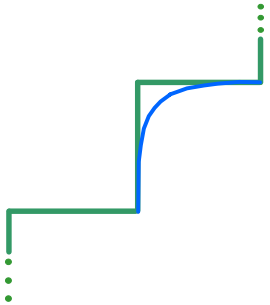


Review from Last Lecture

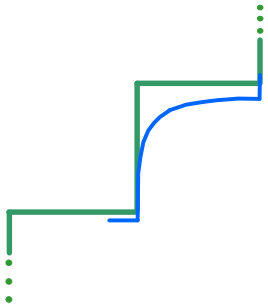
DAC Performance Issues and Concerns



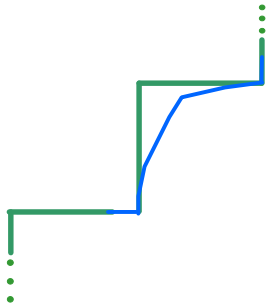
Ideal



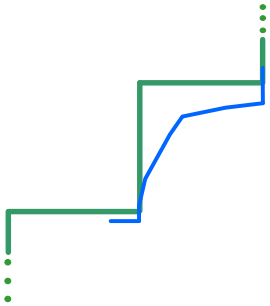
Complete
Linear Settling



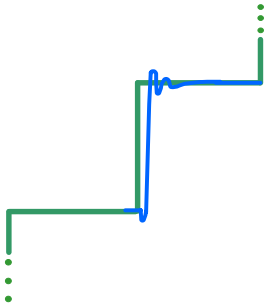
Incomplete
Linear Settling



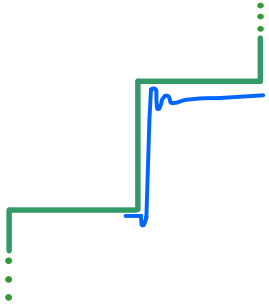
Complete Nonlinear
Settling



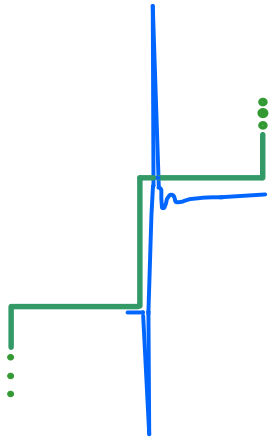
Incomplete
Nonlinear Settling



Complete with glitch



Incomplete with
glitch



Incomplete with big
glitch

Review from Last Lecture

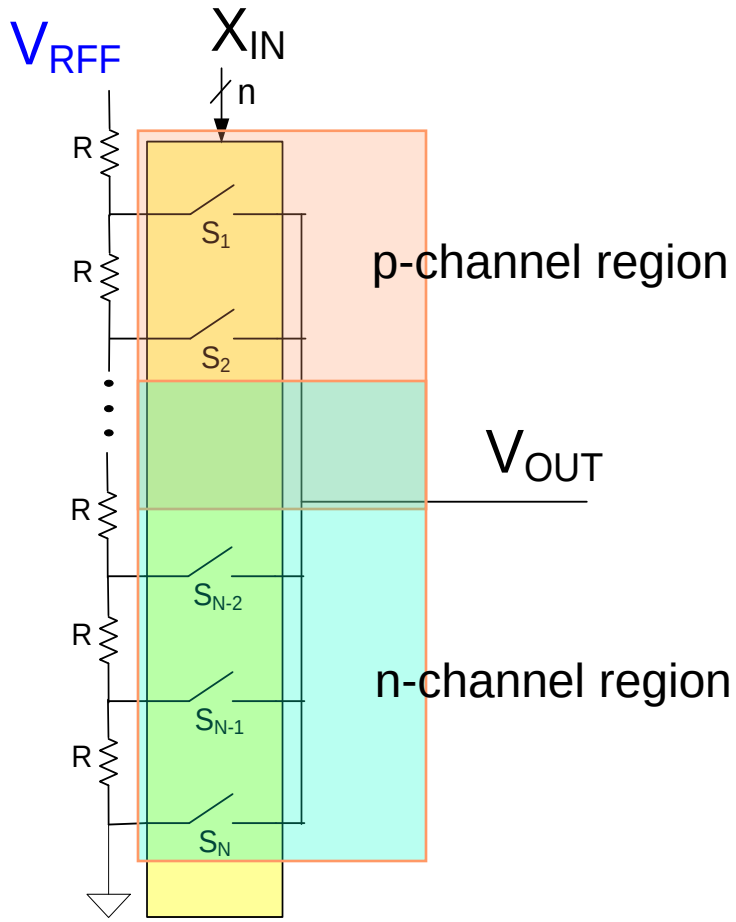
What DAC Architectures are Actually Used?

Listing from Texas Instruments March 1 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

Review from Last Lecture

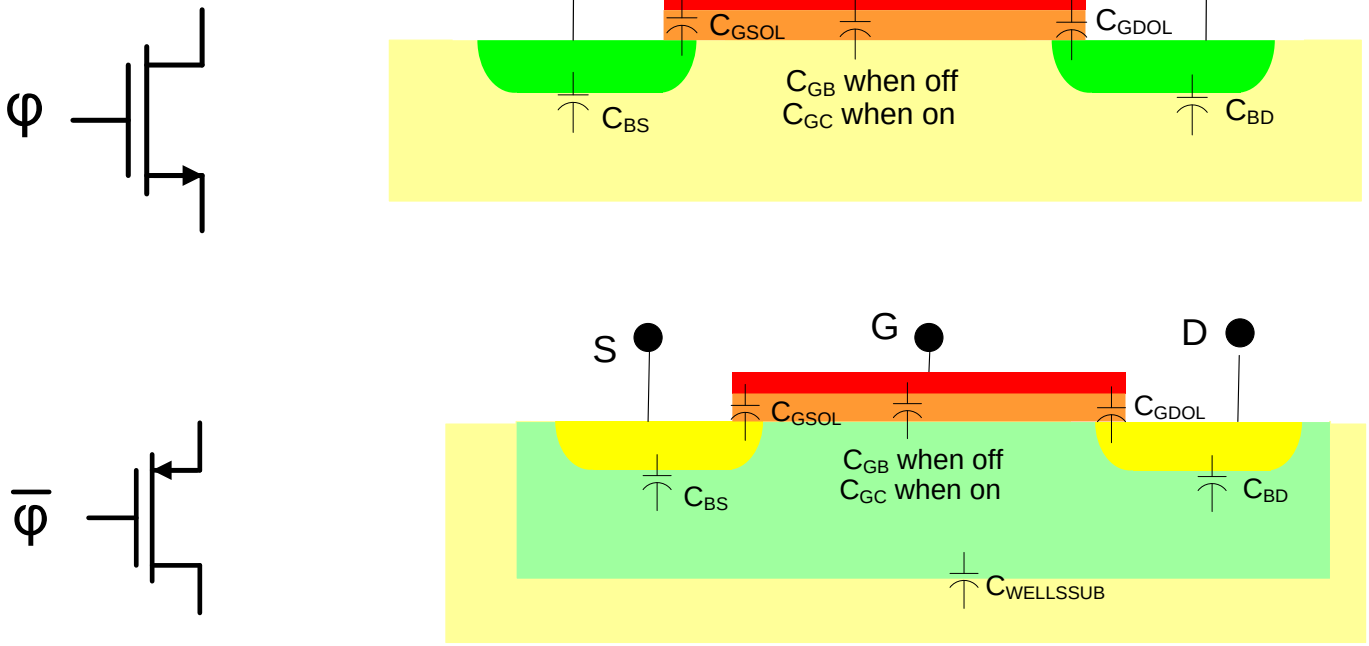
Switch Assignment



Challenges:

Review from Last Lecture

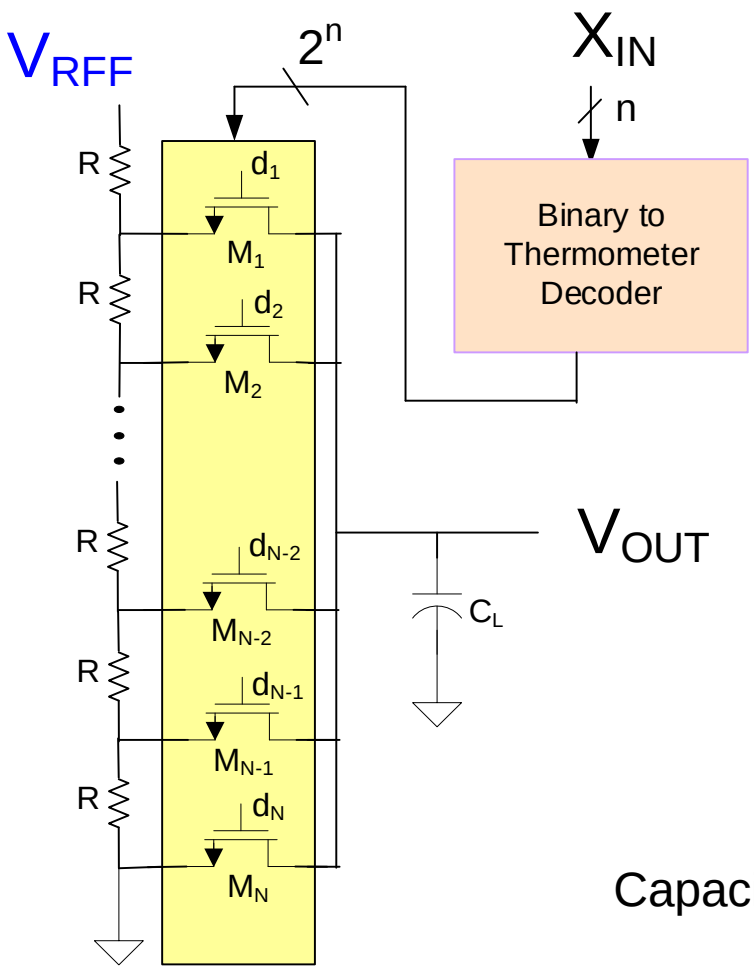
Switch Parasitics



- C_{BD} and C_{BS} can be significant and cause rise-fall times to be position dependent
- C_{GDOL} can cause “kickback” or feed-forward
- C_{GS} can slow turn-on and turn-off time of switch

Review from Last Lecture

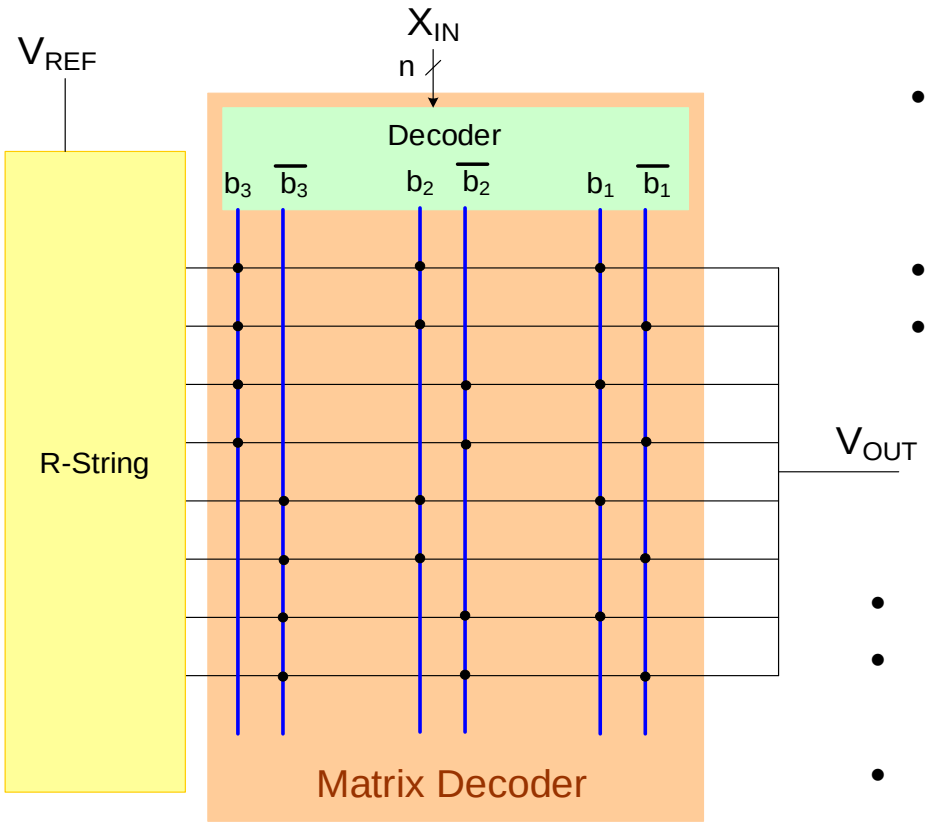
R-String DAC



Capacitive loading due to switches

Review from Last Lecture

R-String DAC



- Uses matrix decoder as analog MUX (don't synthesize decoder)
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)

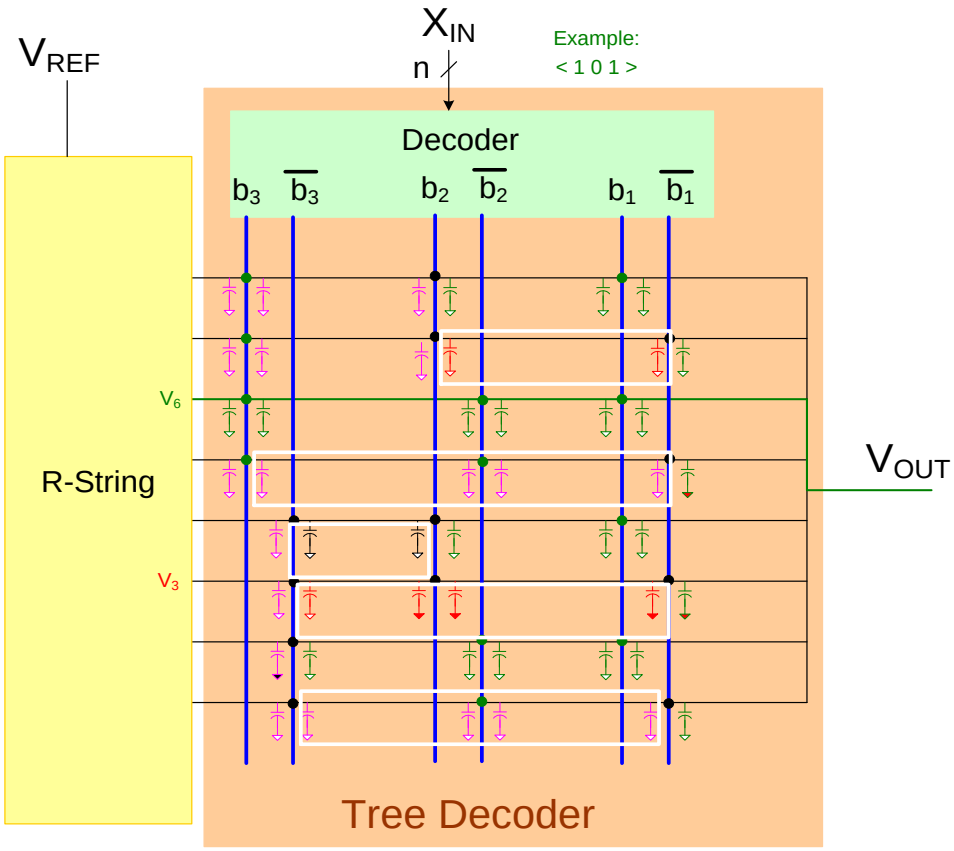
Challenges

- Still many signals to route
- Large capacitance on V_{OUT} (over 2^{n+1} diff caps)
- Multiple previous code dependencies cause output transition time to be quite unpredictable
- Considerable transients introduced on R-string

R-String DAC

Transition from <010> to <101>

White boxes show capacitors dependen
upon previous code <010>

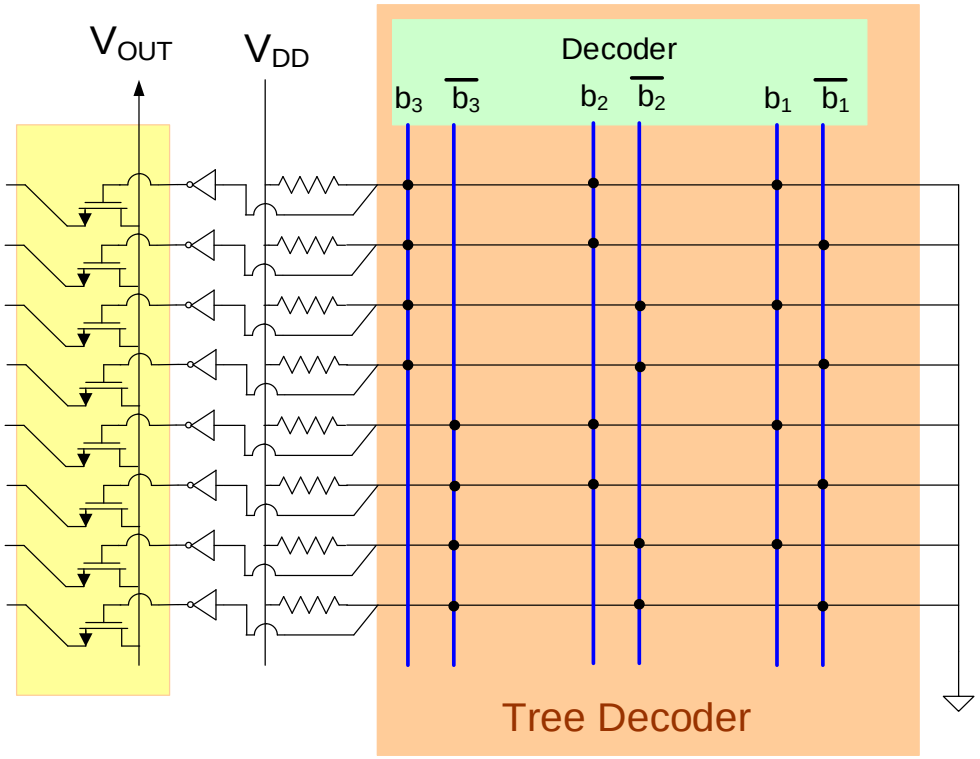


Previous-Code Dependent Settling

- Assume all C's (except those on the R-string) were initially at 0V
- Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage
- Some capacitors may retain values from a previous input for many clock cycles for some inputs resulting I previous-previous dependence of even longer

Review from Last Lecture

R-String DAC



Tree-Decoder in Digital Domain

Single transistor used at each marked intersection for PTL AND gates

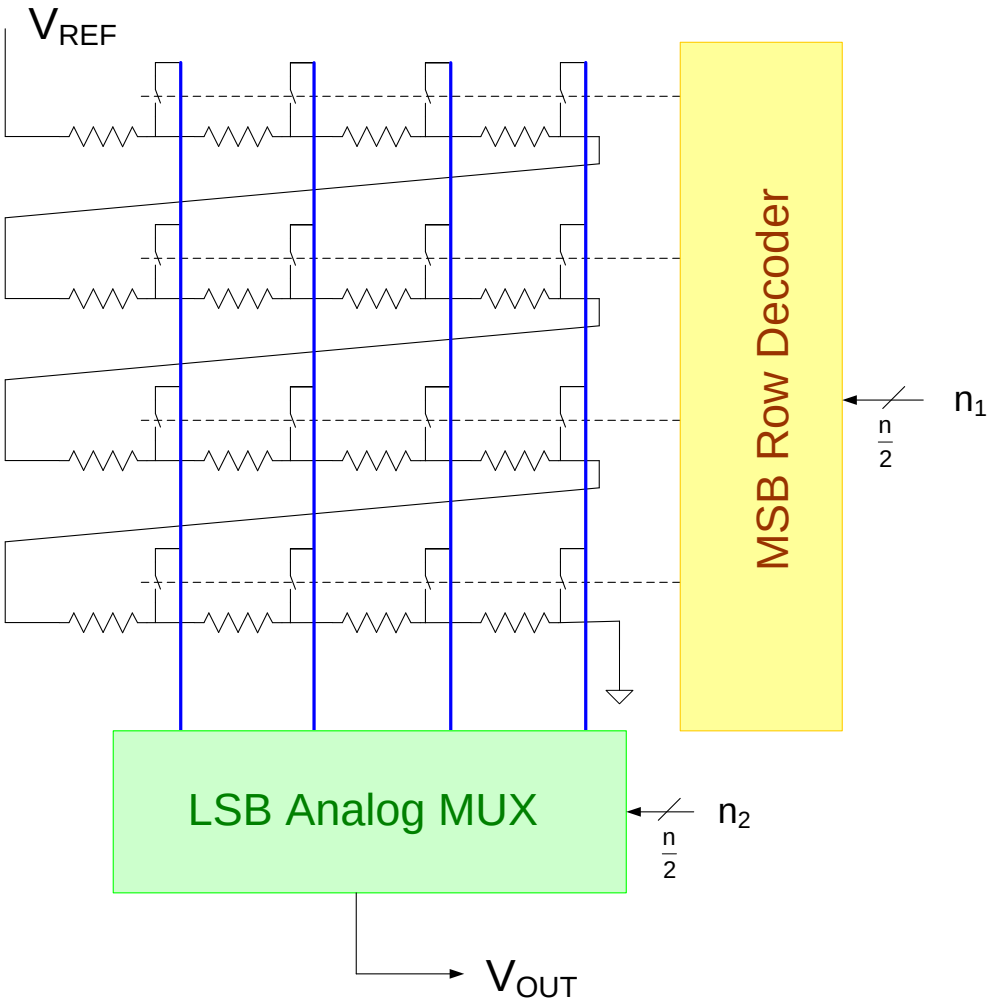
Significant reduction in capacitive loading at output

Do the resistors that form part of PTL dissipate any substantial power?

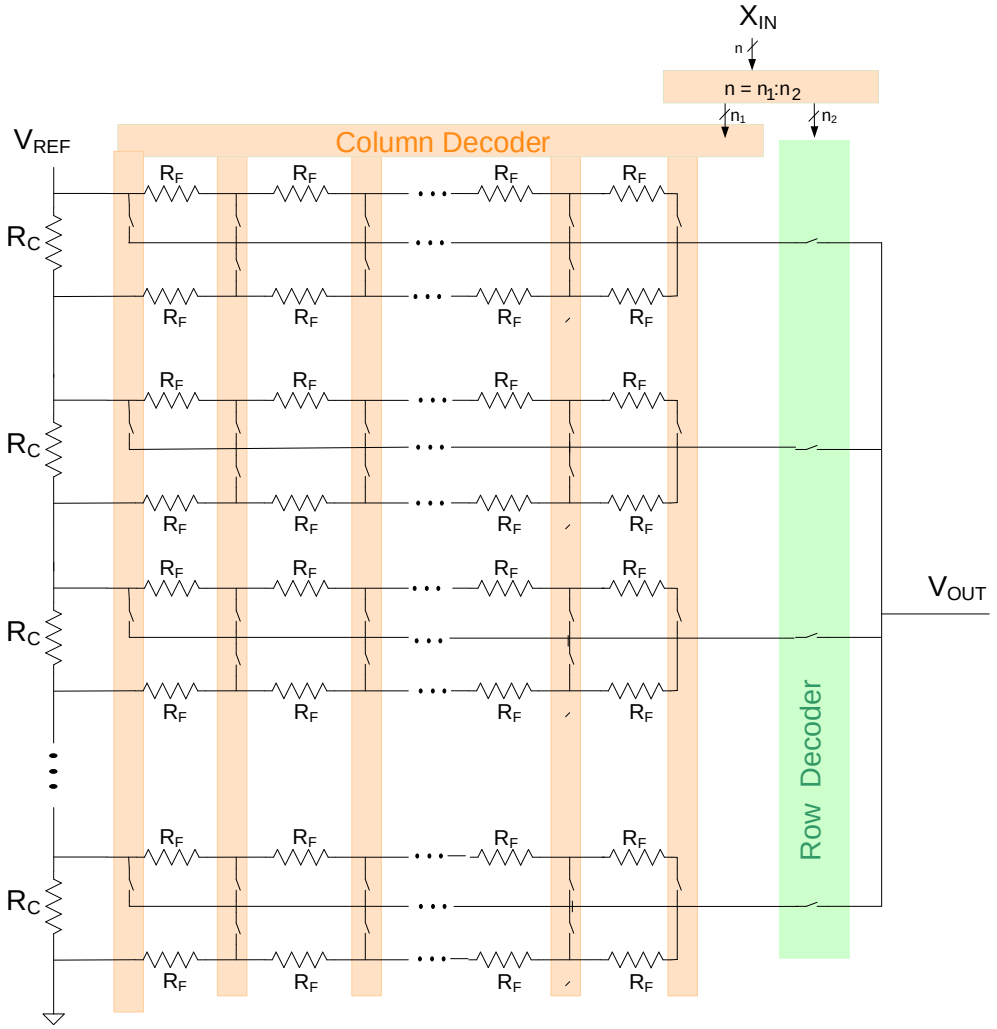
No because only one will be conducting for any DAC output

Will become more complicated if both p-channel and n-channel switches needed

R-String DAC



R-String DAC



Note Dual Ladder is used !

A 10-b 50-MHz **CMOS D/A** converter with 75-ω buffer

MJM **Pelgrom** - Solid-State Circuits, IEEE Journal of, 1990 - ieeexplore.ieee.org

Abstracf-A 10-b 50-MHz digital-to-analog (D/A) converter is pre-sented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, ...

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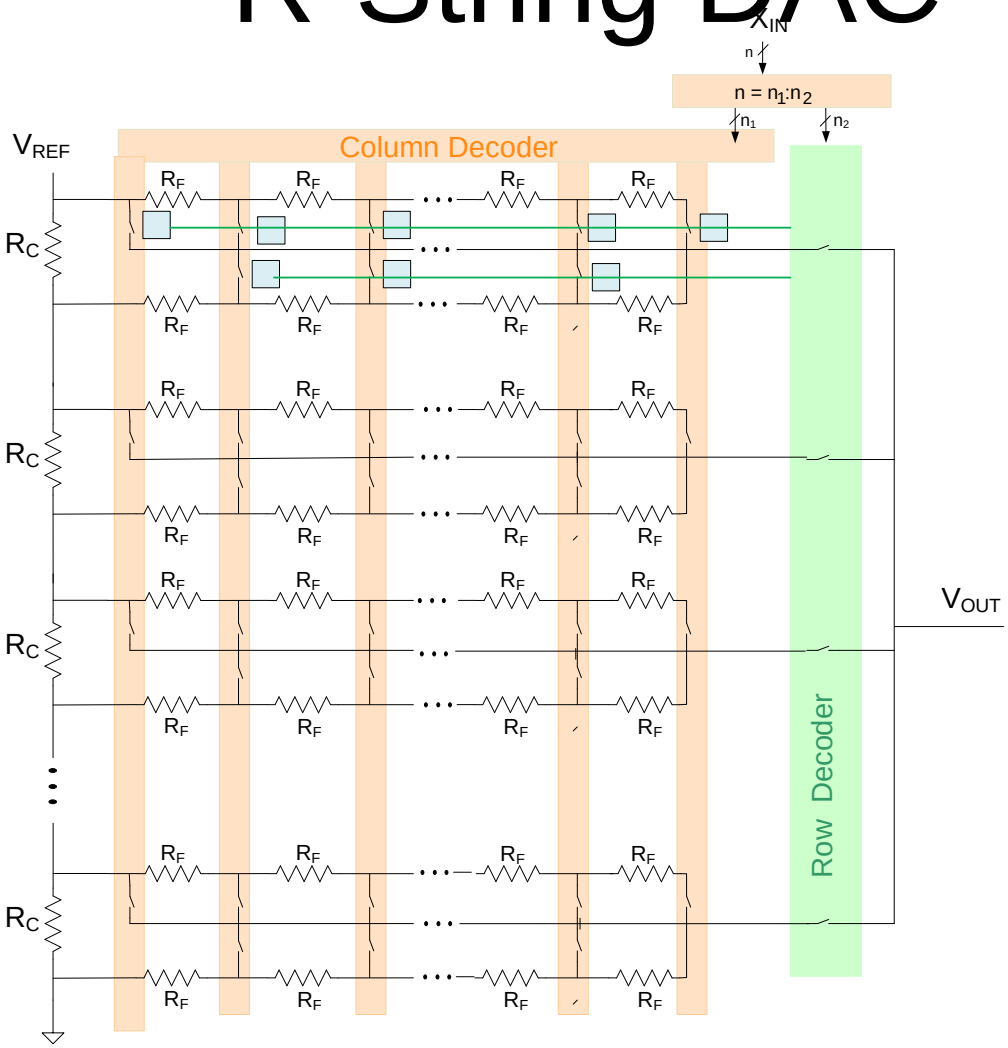
R-String DAC



Note Dual Ladder is used !

□ : AND pixel sensor gate

32x32 Matrix

A 10-b 50-MHz **CMOS D/A** converter with 75-ω buffer

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A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer - Get It@ISU

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Cited by 94 (4/6/14) Cited by 133 (3/8/21)

A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

MARCEL J. M. PELGROM, MEMBER, IEEE

Abstract —**A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, and signal-dependent switch signals reduce high-frequency distortion. The output buffer allows driving 1 V_{pp} to 75 Ω. The chip consumes 65 mW at *maximum clock frequency and a full-swing output signal*. The device is processed in a standard 1.6-μm CMOS process with a single 5-V supply voltage.**

Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter

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Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter intended for supplying 1 V_{pp} to 75 Ω will consequently require 80-mA power supply current.

This paper proposes a trimless 10-b 50-MHz D/A converter based on resistor strings. This D/A converter is well suited to be used together with nearly all reported A/D converters for high speed, as these also use resistor strings to obtain the reference for the comparators. The design improves on the standard single-resistor-string approach by using a dual-ladder architecture [3] in a matrix formation [4], [5]. Several measures have been taken in the ladder to reduce the distortion. The decoding aims at minimizing the number of transistors that switch. The on-chip output buffer allows driving 1 V_{pp} to 75 Ω. The inherent voltage output allows driving a two-sided terminated transmission line with a better power efficiency than a current cell D/A converter.

Section II presents the design considerations and chip architecture and Section III shows some measurements on the device. The work is summarized in Section IV.

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II. The Chip Design

A. The Ladder Structure

The voltage dependence and the mutual matching of large-area polysilicon resistors allow the design of a converter with high integral and differential linearity. Basically, the variation in the polysilicon resistance value is determined by its geometry variations: the length and width variations result in local mismatches and the thickness variation gives gradients. Equally sized MOS gates suffer in addition to charge variations in the threshold voltage. However, the design of the D/A converter with a single 1024-tap resistor ladder and sufficiently fast output settling requires tap resistors in the order of 6–10 Ω. The size of such resistors in conventional polysilicon technology is such that accurate resistor matching and consequently linearity become a problem.

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The solution to this problem is the combination of a dual ladder [3] with a matrix organization Randy Geiger Fig. 1 shows the ladder structure. The coarse ladder consists of two ladders each with 16 large-area resistors of 250 Ω which are connected anti-parallel to eliminate the first-order resistivity gradient. The coarse ladder determines 16 accurate tap voltages and is responsible for the integral linearity. A 1024-resistor fine ladder is arranged in a 32-by-32 matrix, where every 64th tap is connected to the coarse-ladder taps. This arrangement allows the fine-ladder tap resistance to be increased to 75 Ω without loss of speed. The effect of wiring resistances has to be related to the 75-Ω tap resistors and can therefore be neglected. There are only currents in the connections between the ladders in the case of ladder inequalities: this reduces the effect of contact resistance variance. The current density in the polysilicon is kept constant to avoid field-dependent nonlinearities. The coarse ladder is designed with polysilicon resistors in order to avoid voltage dependence of diffused resistors. The fine ladder is designed either in polysilicon or diffusion, depending on secondary effects in the process implementation.

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and therefore reduces the odd harmonics. In this design, partial cancellation was achieved by placing a unity resistor at the appropriate positions in the output rail. The use of unity resistors keeps the layout simple and does not require additional chip area.

The second source of the varying output impedance is the switch transistor. Usually its on-state gate voltage equals the positive power supply; the voltage on its source terminal, however, is position dependent. The turn-on voltage doubles from one end of the ladder to the other. In this design an additional supply ladder is placed on top of the signal ladders to keep the turn-on voltage of the switches more constant. Effectively the turn-on voltage of each switch transistor is made equal to the lowest turn-on voltage of a basic ladder D/A structure. Therefore there are no additional power supply constraints. For an easy implementation, the switches along each output rail have a common supply line. The variation in turn-on voltage is thereby reduced by a factor of 16. The upper group of switches is fed from the power supply while each lower group is fed with a voltage lowered by one-sixteenth of the maximum signal swing. An additional advantage of this compensation is that the impedance of the switch can be in the order of the total ladder resistance: the switches reduce in width and consequently the clock feedthrough is also reduced.

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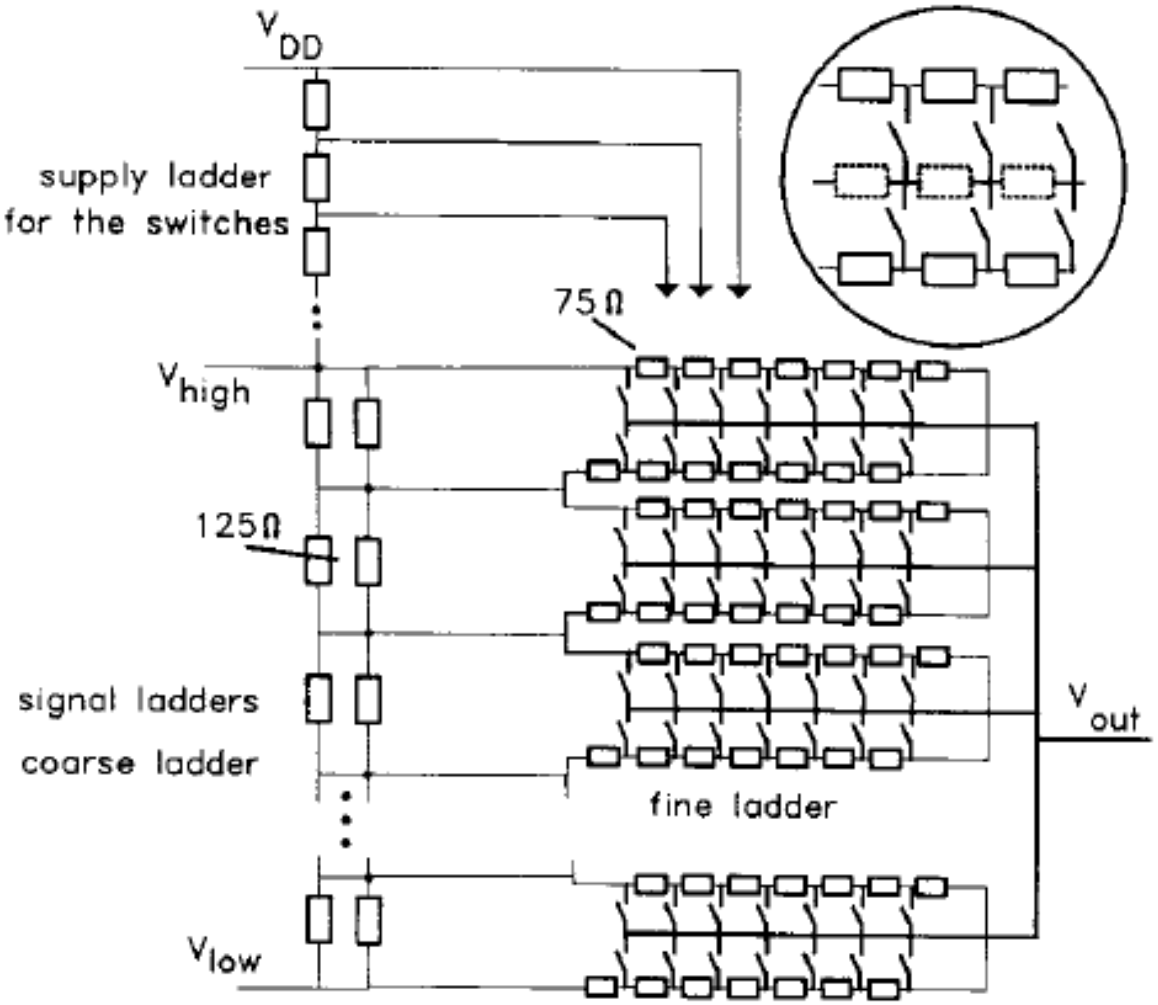

Fig. 1. Resistor network for the video D/A converter.

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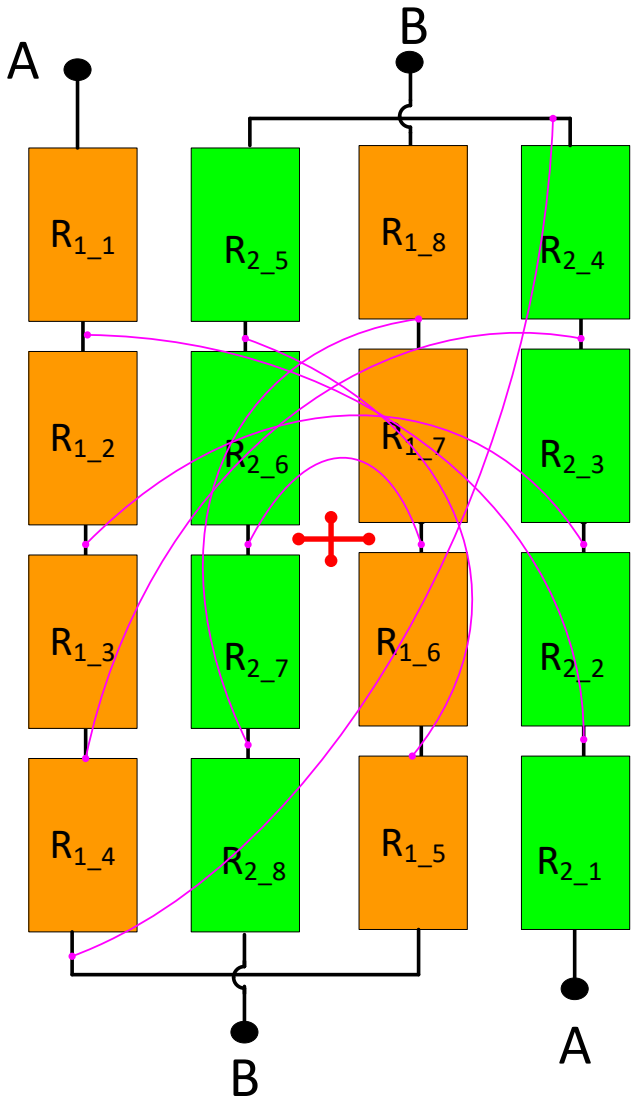
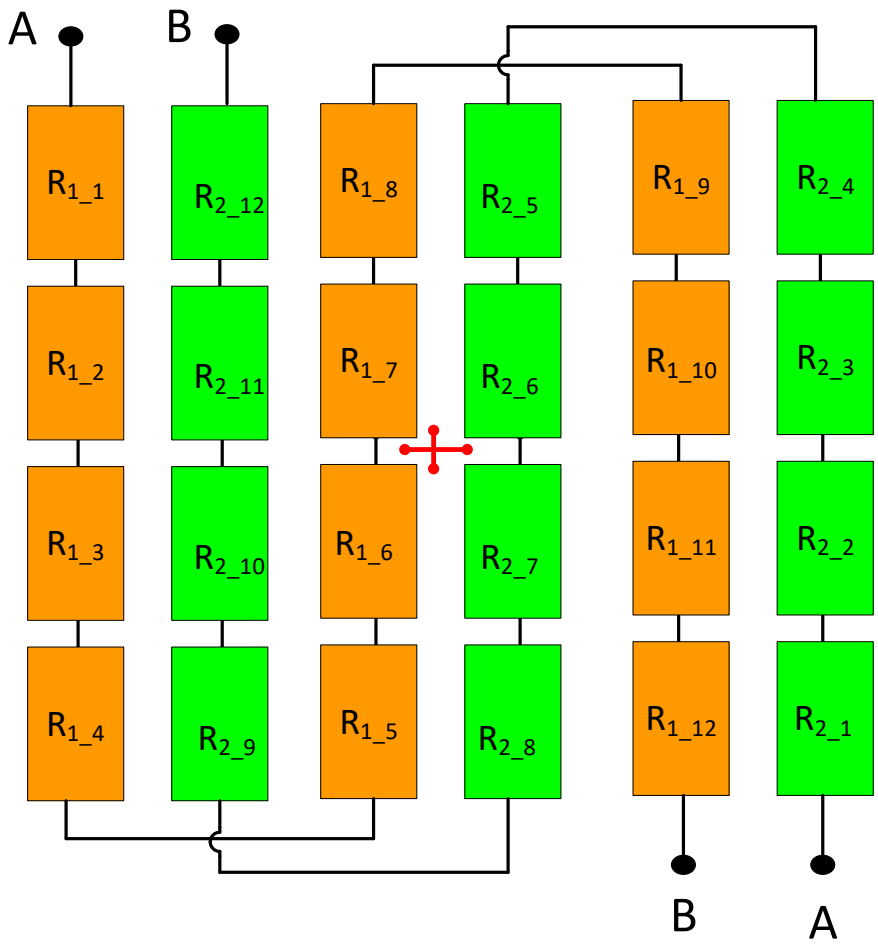
In a basic ladder design consisting of one string of 1024 resistors, the output impedance of the structure varies with the selected position on the ladder and therefore with the applied code. The varying output impedance in combination with the load capacitance results in unequal output charging time and consequently signal distortion of high-frequency output signals. This source of varying impedance has been eliminated by means of a resistive output rail. The insert in Fig. 1 shows a part of two rows of the matrix. Small resistors are placed in the output rail which connects the switches together. These resistors can be chosen in such a way that any path from the beginning of the resistor row to the end of the output rail shows the same impedance, independent of the chosen switch. This eliminates position-dependent charging of the output rail

Common-Centroid Anti-Parallel Ladder Layout



Common-Centroid Anti-Parallel Ladder Layout



Interconnects Not Shown

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B. The Digital Decoder

The core of the D/A converter is formed by the 32-by-32 fine-resistor matrix. A switch and a two-input AND gate[1] are connected to each fine resistor to form a basic cell. Two rows of 32 cells each are arranged around one output rail to form one of the 16 sections of the 10-b D/A converter (see Fig. 2). In operation one of the tap voltages of the fine ladder is switched to one of the 16 output rails of the matrix and subsequently to the input of the buffer. In order to select the proper switch, the 10-b digital input word is split in two 5-b words which are decoded by two sets of 5-to-32 decoders, as shown in Fig. 2. The 5-to-32 decoding is performed in two steps: a predecoder converts into ten lines that control 32 three-input NOR gates of which one gate is activated. In this way minimum capacitive load is driven and maximum speed is achieved. The two decoders are placed on two sides of the matrix. The two sets of 32 decoded lines are latched by the main clock before running horizontally and verti-

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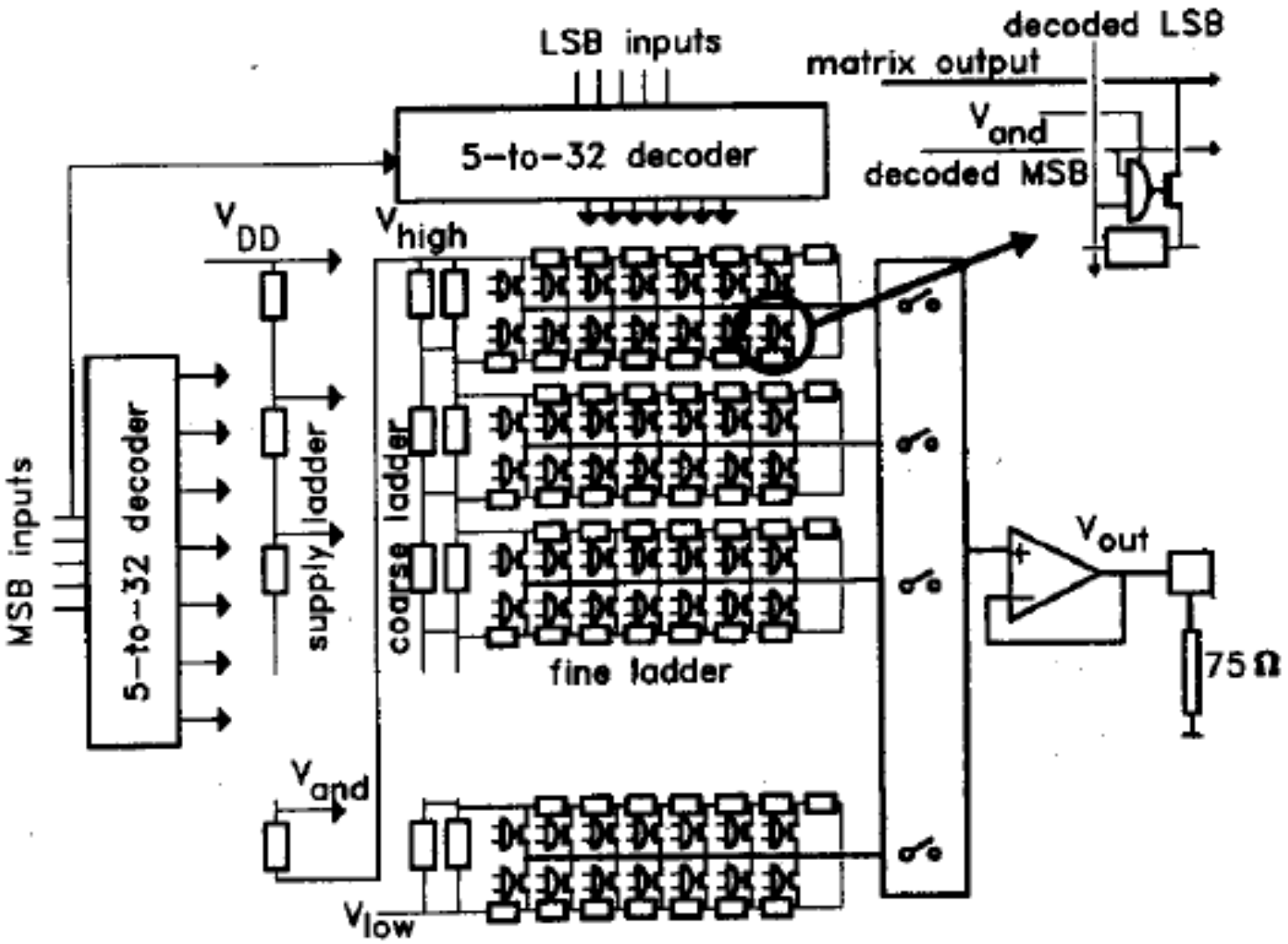
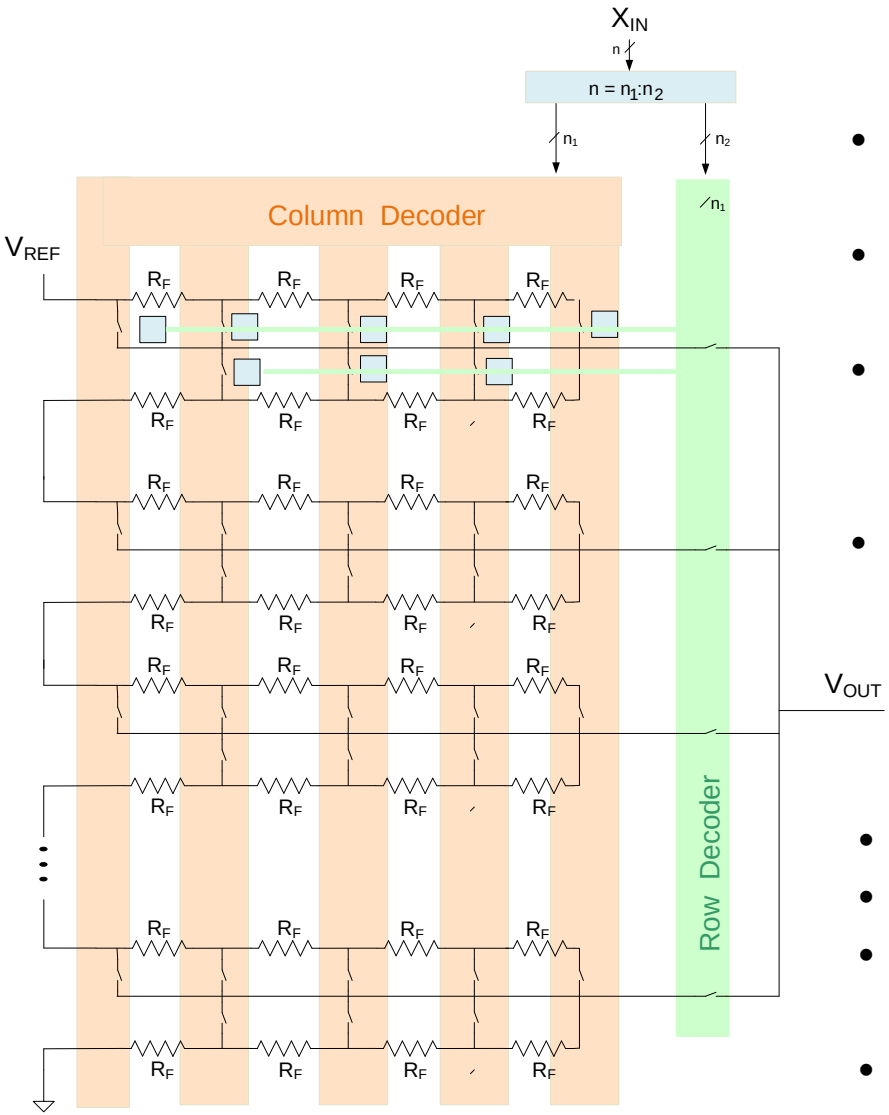


Fig. 2. Block diagram of the D/A converter.

R-String DAC

String DAC with Row-Column Decoder



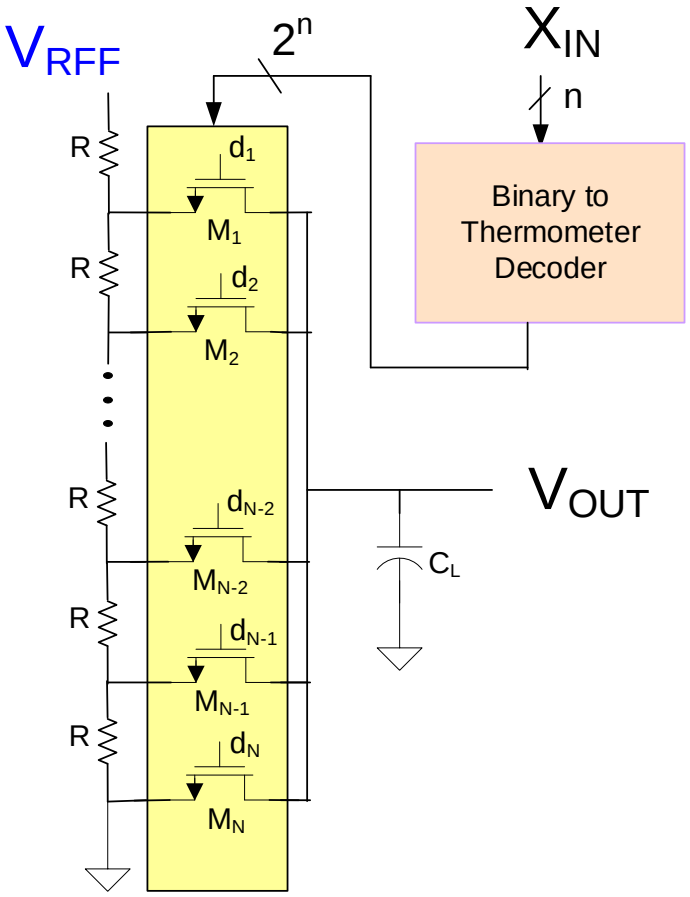
- Dramatic reduction in decoder complexity
- Dramatic reduction of capacitive loading on output
- Changes decoder from a one-dimensional to a two-dimensional solution (can be thought of as folding)
- Logic gates could be placed at each node to eliminate analog row decoder

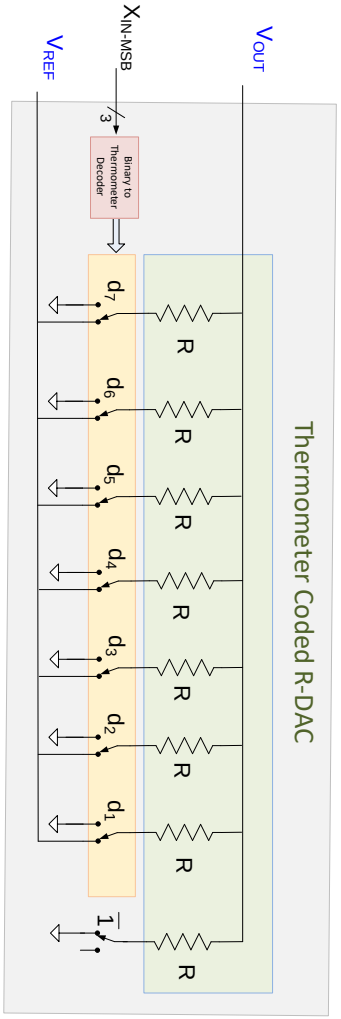
Challenges (most were present in earlier structures too)

- Some previous code dependence
- INL large
- Difficult to cancel gradient effects in layout

  Switching sequencing can help a lot
- Switch impedances code dependent
- Settling times code dependent

R-String vs R-Ladder

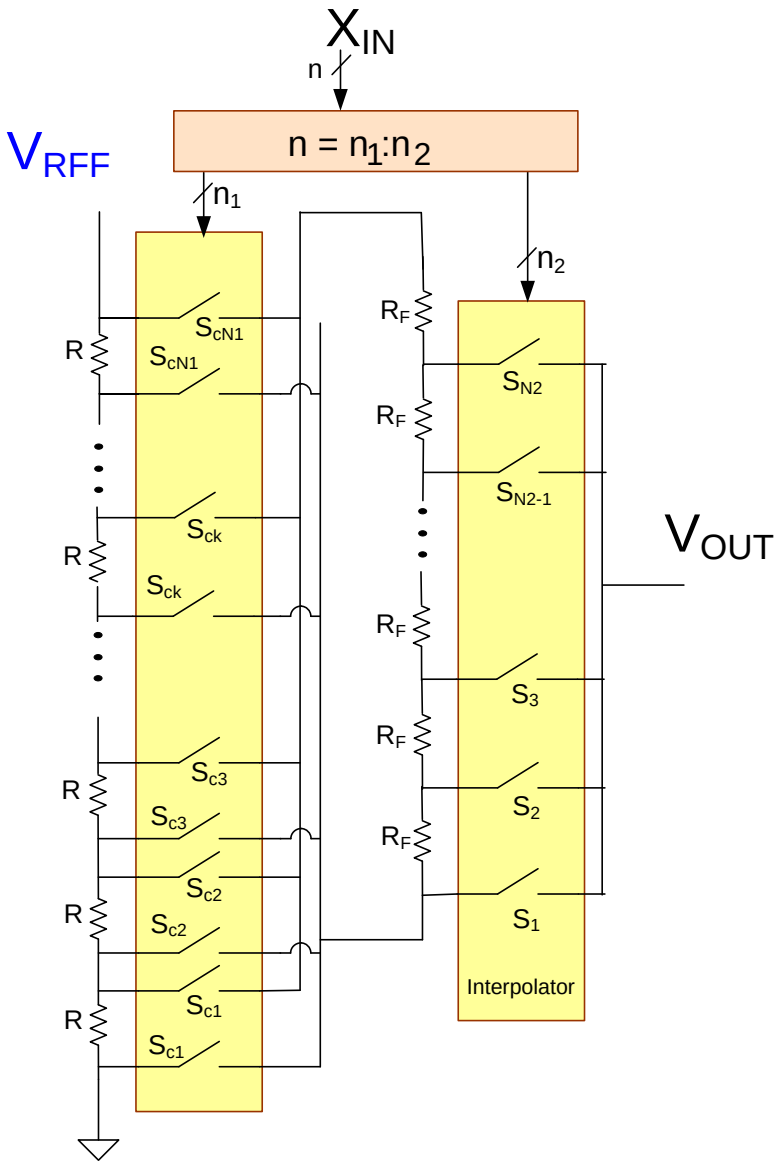




How do these structures compare?

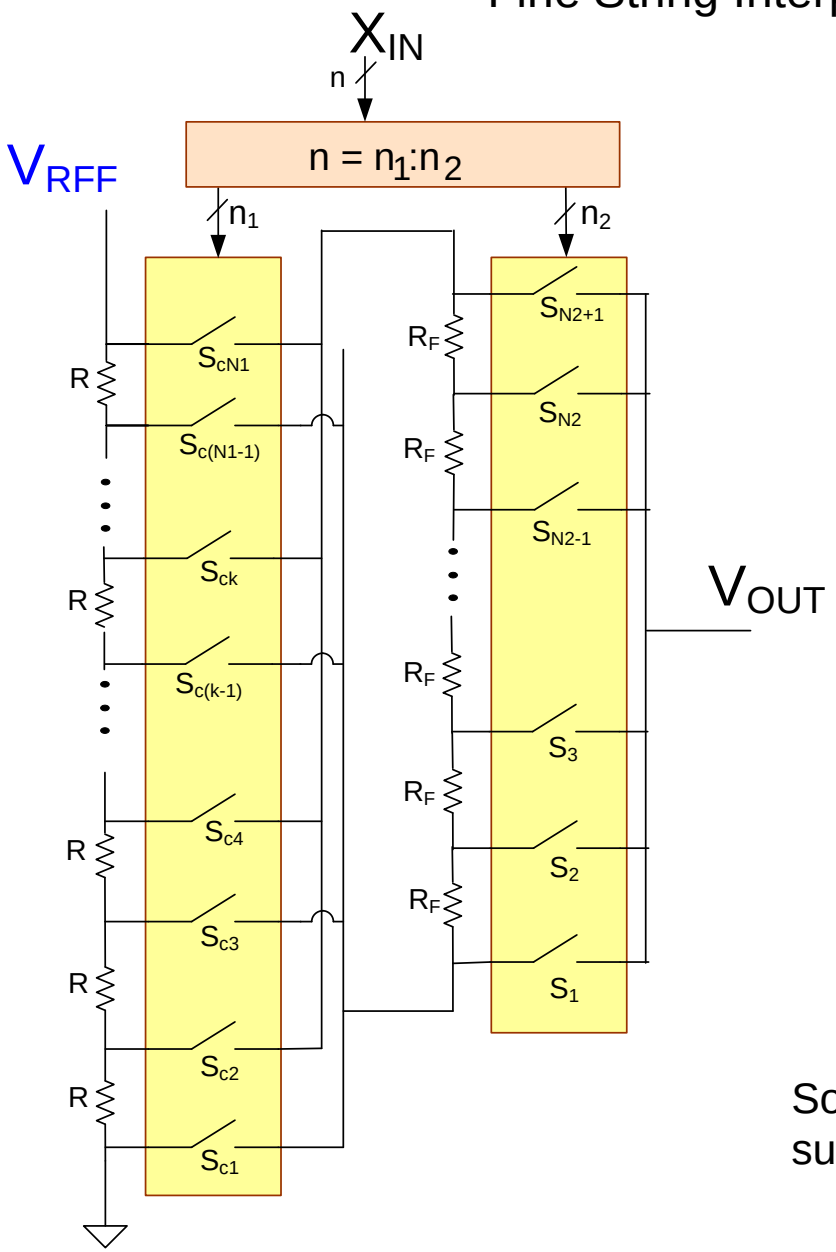
R-String DAC

Fine String Interpolator



R-String DAC

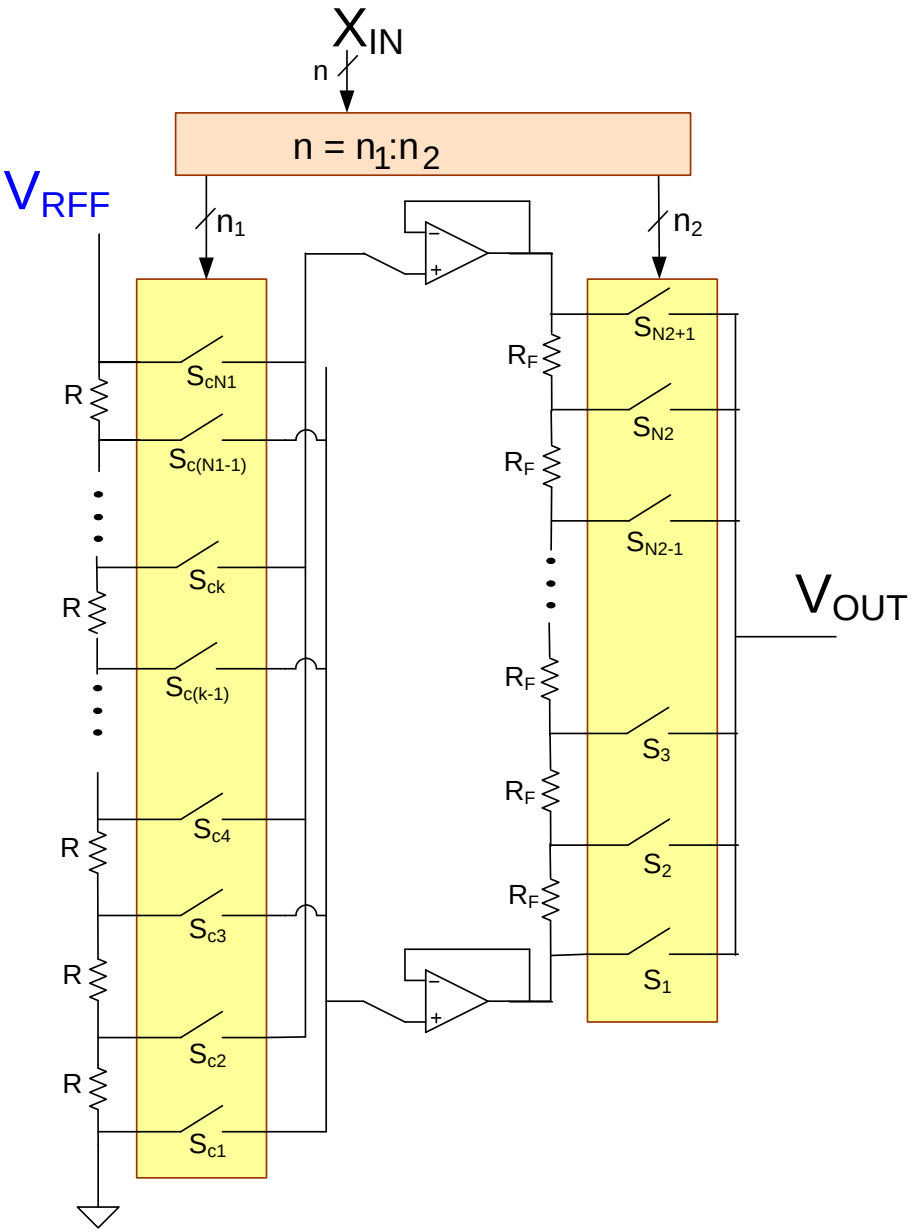
Fine String Interpolator



Sometimes termed sub-divider, sub-range or dual-string DAC

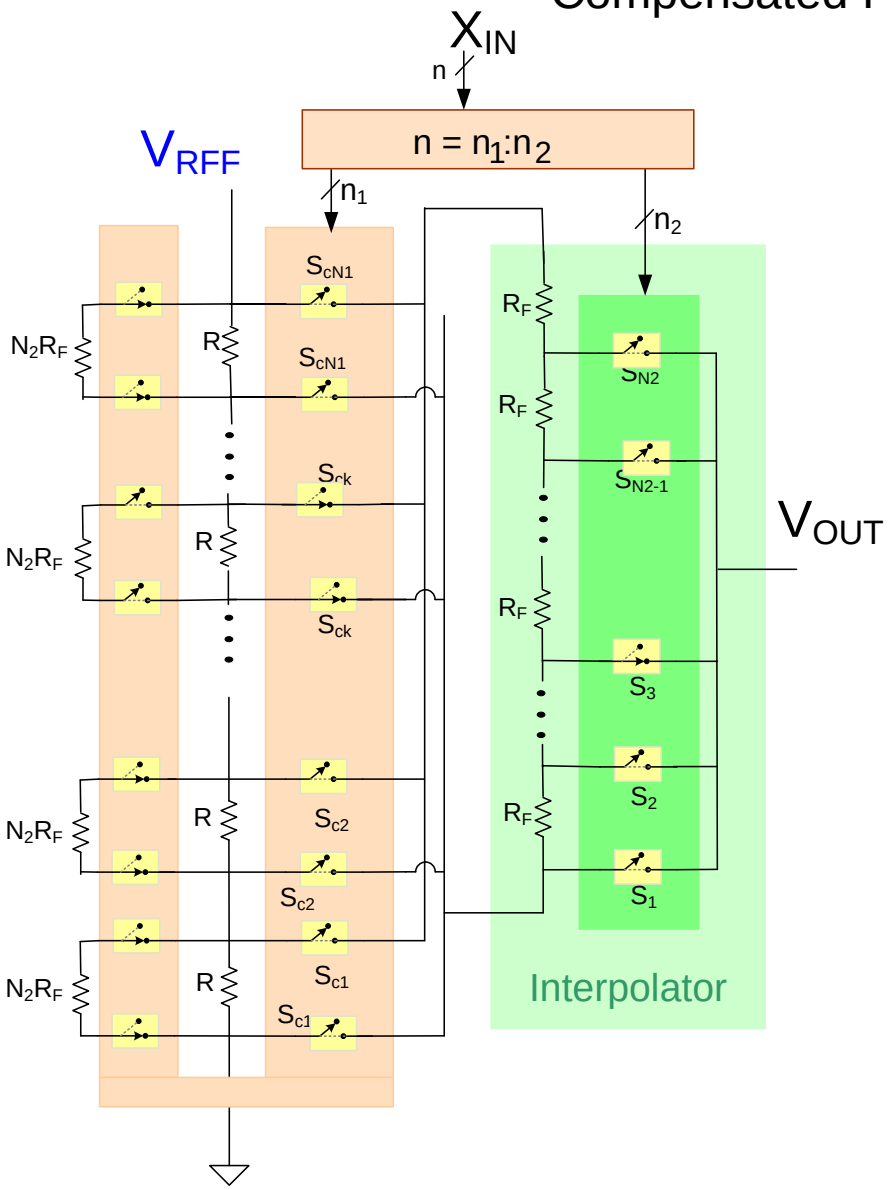
R-String DAC

Buffered Fine String Interpolator



R-String DAC

Compensated Fine String Interpolator



$N_2 = 2^{n_2}$

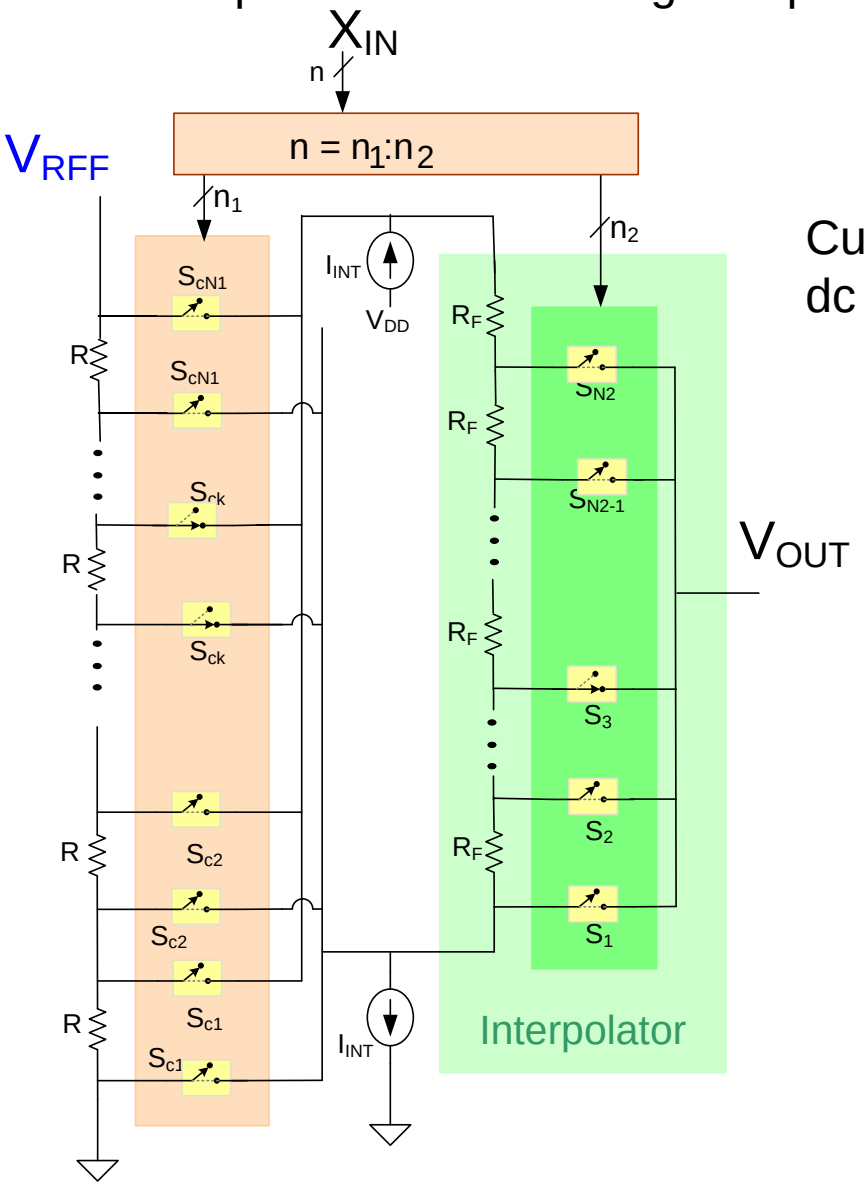
Paralleling each R will be either the interpolator or a resistor of value N_2R_F

Area of N_2R_F resistors may be very small

Tap voltages on coarse R-string should not change with X_{IN}

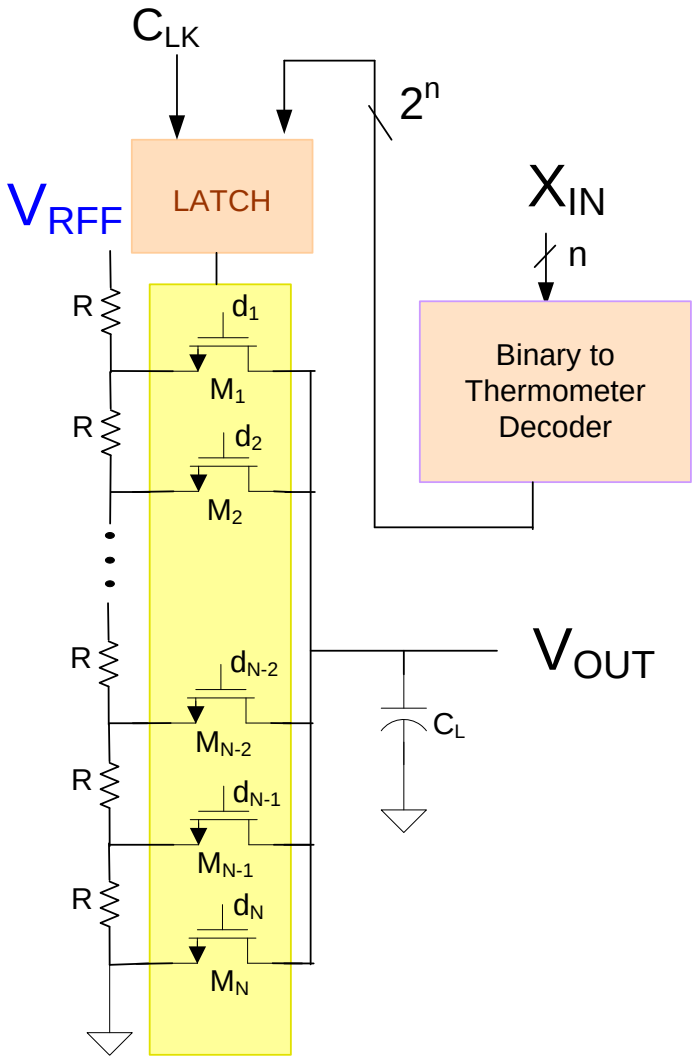
R-String DAC

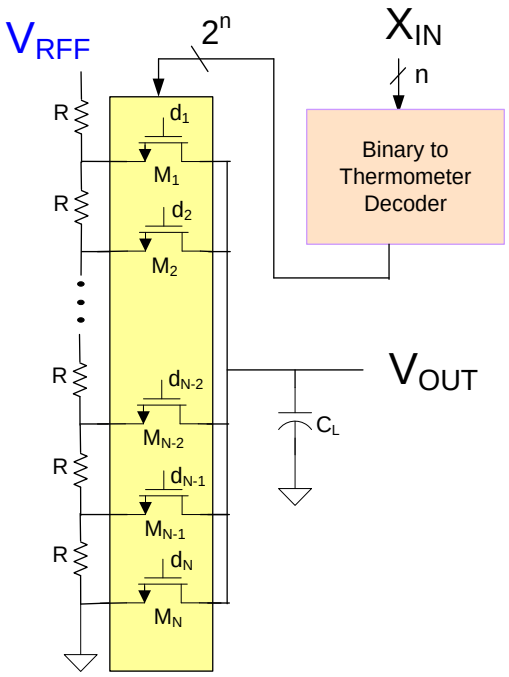
Compensated Fine String Interpolator

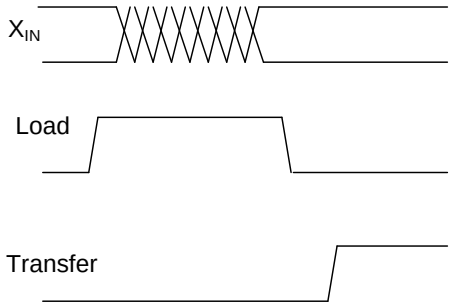


Current Sources have same dc current as interpolator

Basic R-String DAC



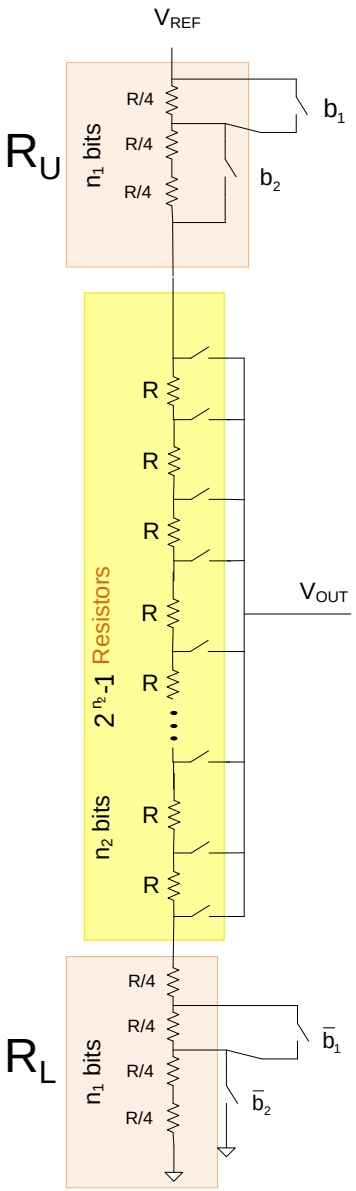




Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion

Basic R-String DAC

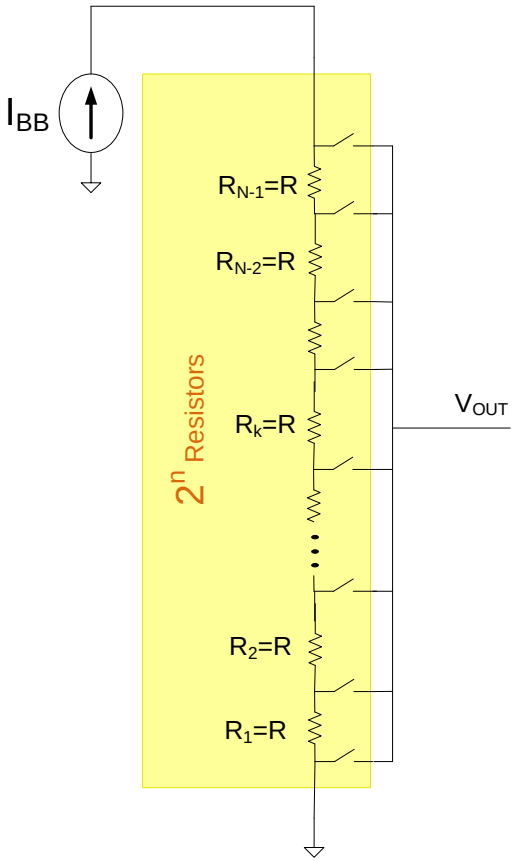
Dither DAC



For all b_1 and b_2, $R_U+R_L=R$

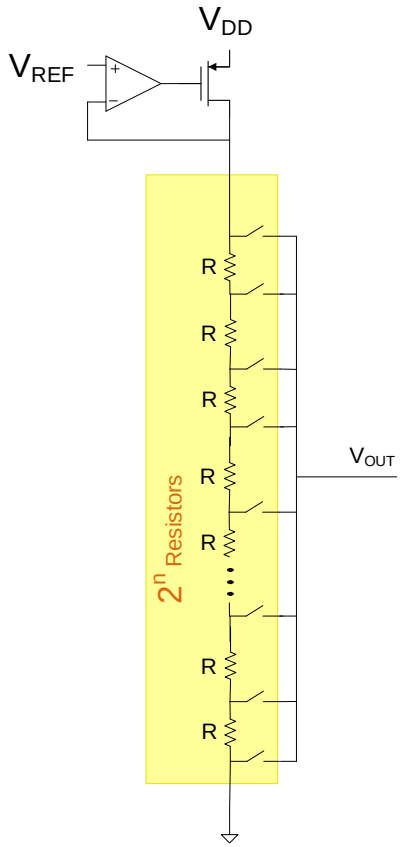
- Another Segmented DAC structure
- Can be viewed as a “dither” DAC
- Often n_1 is smaller than n_2
- Dither can be used in other applications as well

Basic R-String DAC



$$V_{0k} = I_{BB} \bullet \sum_{i=1}^{k} R_k \qquad \text{for } k \geq 1$$

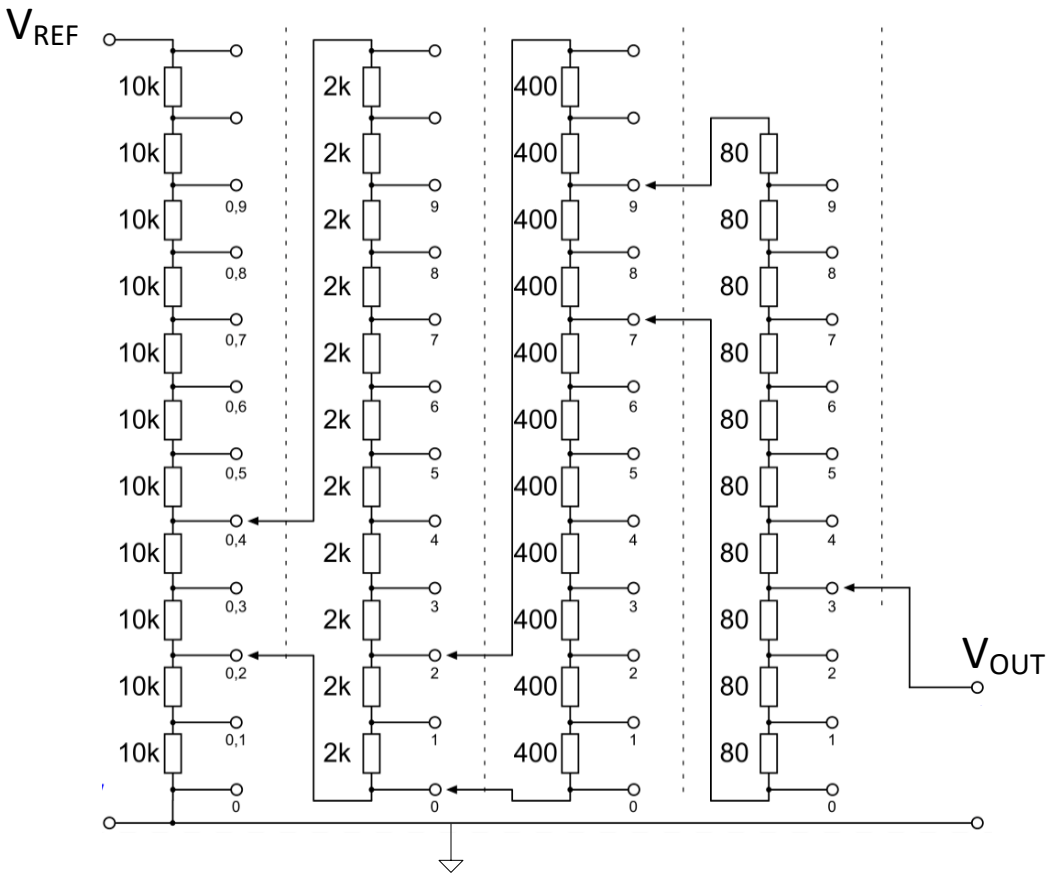
Impedance facing V_{OUT} is code dependent



No loading of V_{REF}
Kickback to V_{REF} removed

Kelvin-Varley Divider

- Shown as decimal divider (1 decimal digit per stage)
- 11 resistors in each string except last which has 10



Requires decoders to control switches but they are small

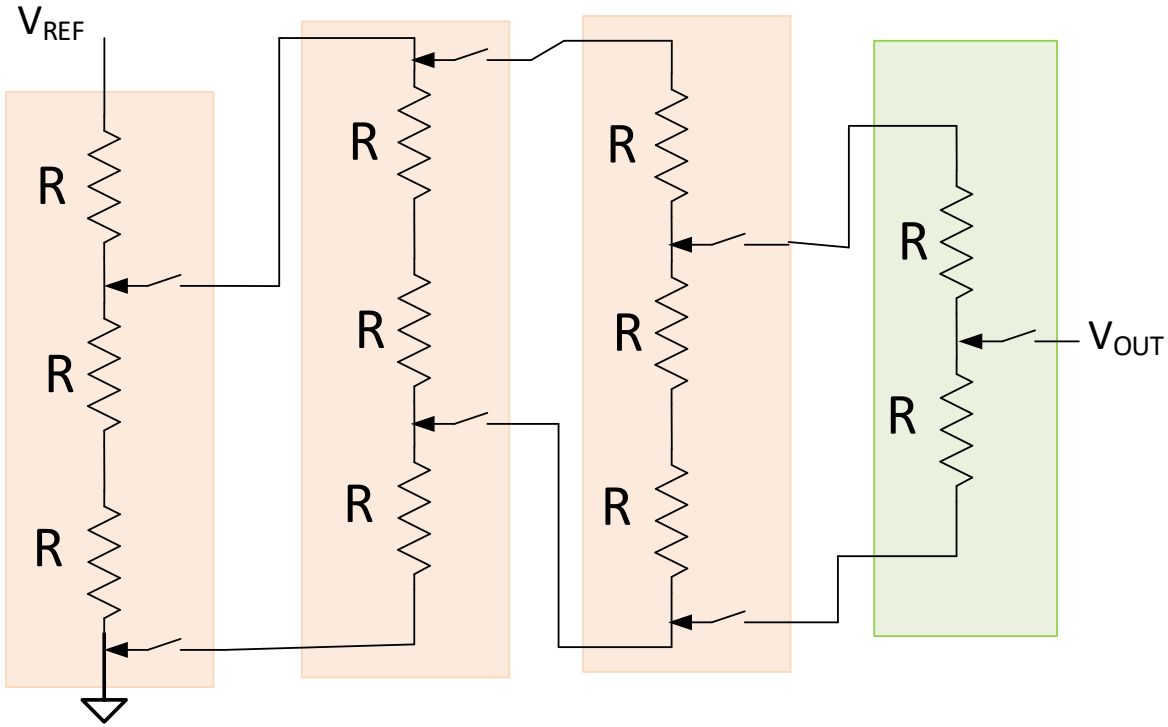
(Artwork modified from Wikipedia)

- **William Thomson, 1st Baron Kelvin (1824-1907)**
- **Cromwell Fleetwood Varley (1828-1883)**

Kelvin-Varley Divider

Concept Can Be Extended to Any Base

- Shown as binary divider (1 bits/stage)
- 3 resistors in each string except last which has 2

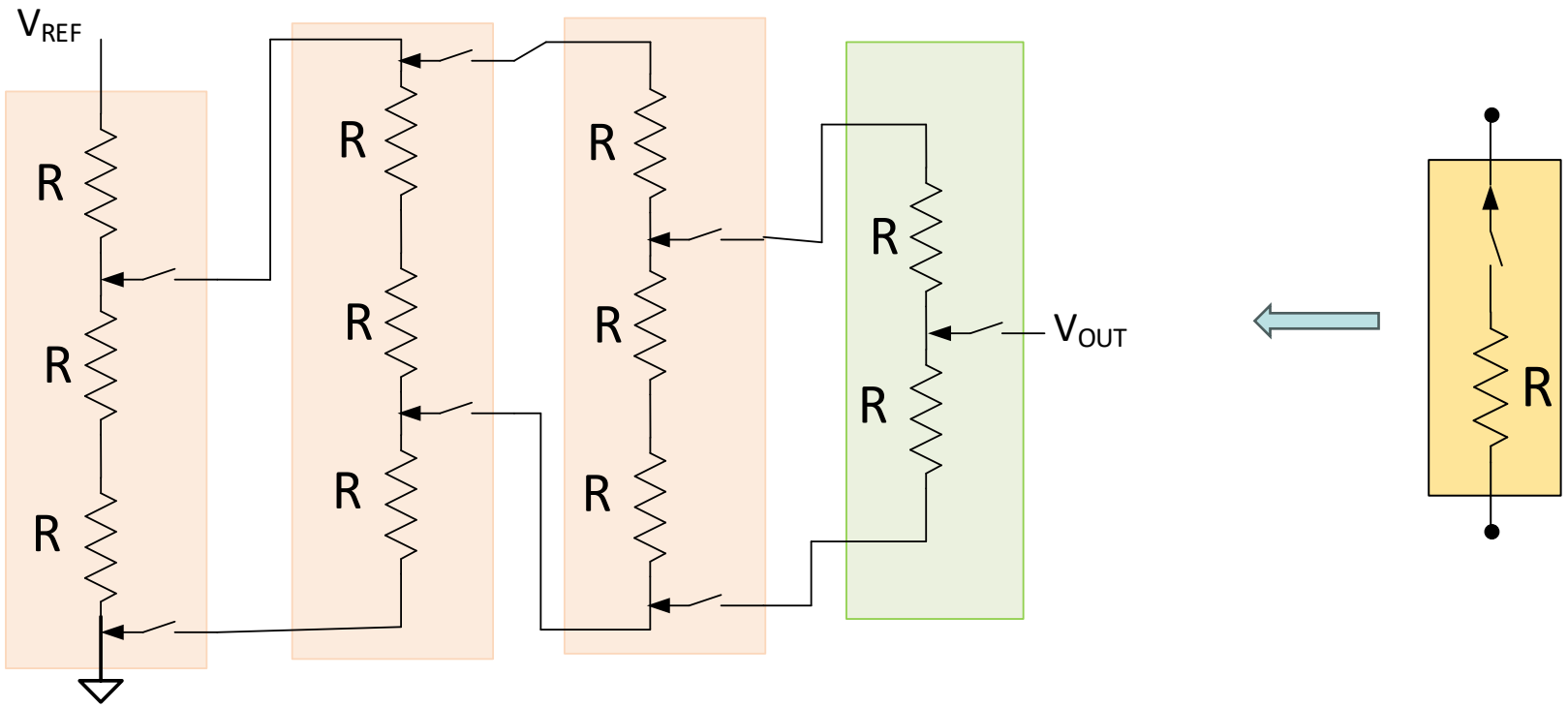


No decoder needed to control switches

Kelvin-Varley Divider

Concept Can Be Extended to Any Base

- Shown as binary divider (1 bits/stage)
- 3 resistors in each string except last which has 2



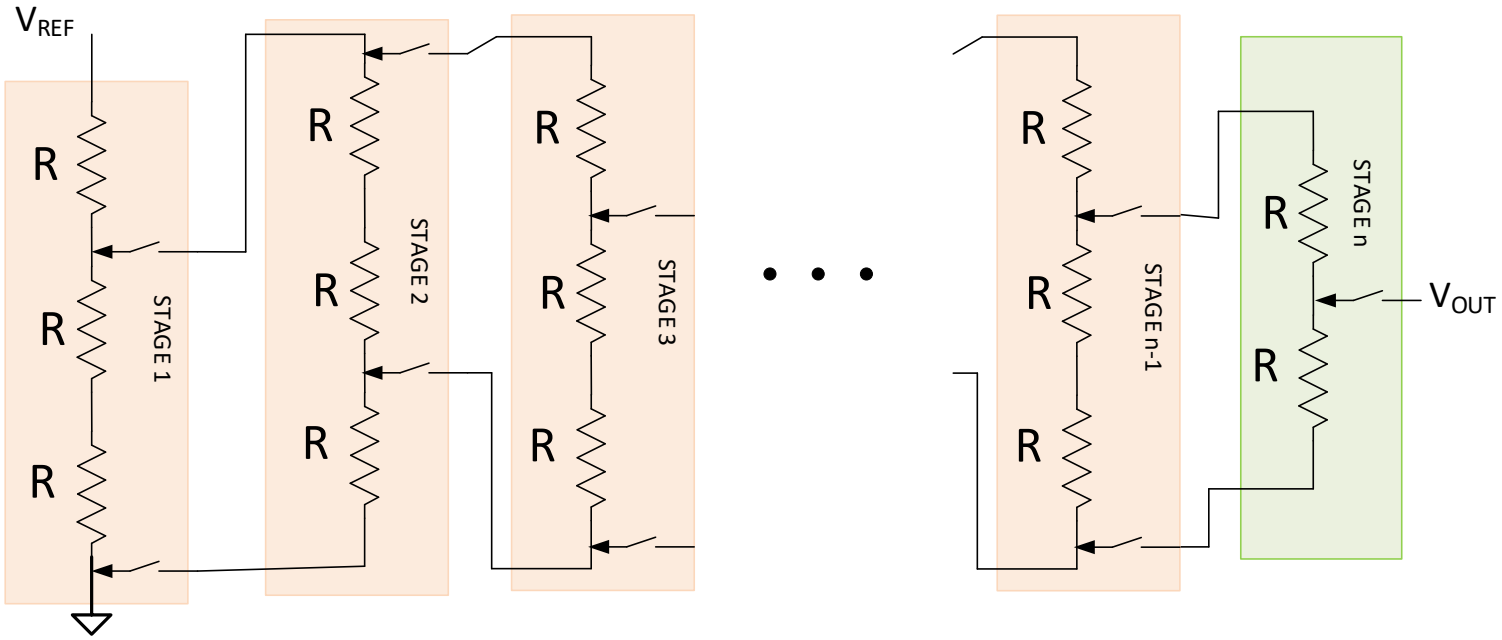
Switch Impedance Degrades Performance (Much like R-2R)

Can we make each resistor as a unary resistor-switch cell to compensate for switch impedance?

Kelvin-Varley Divider

Concept Can Be Extended to Any Base

- Shown as binary divider (1 bits/stage)
- 3 resistors in each string except last which has 2
- Can be extended to any number of stages

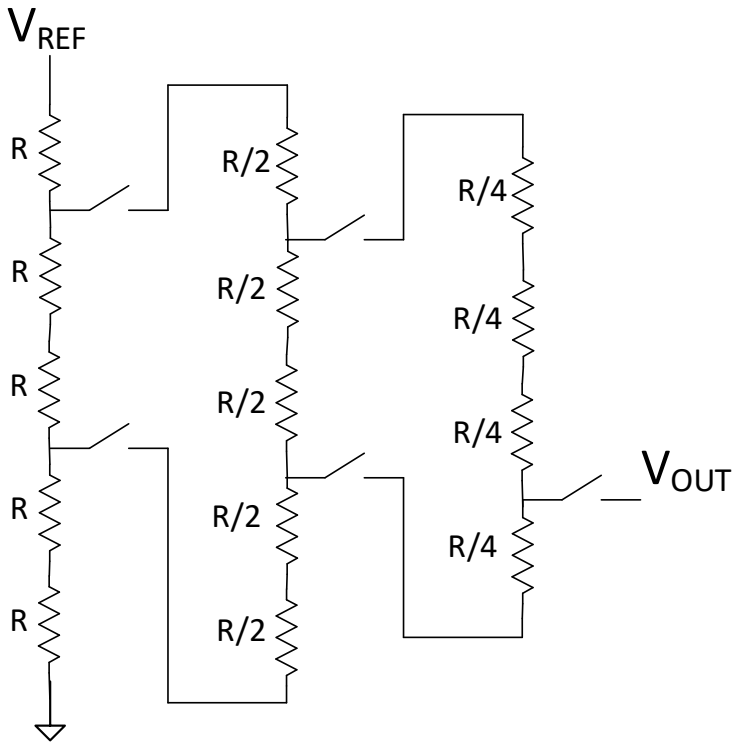


No decoder needed to control switches
All resistors of same value
Physical size of resistors need not be the same

Kelvin-Varley Divider

Concept Can Be Extended to Any Base

- Shown as binary divider (2 bits/stage)
- 5 resistors in each string except last which has 4

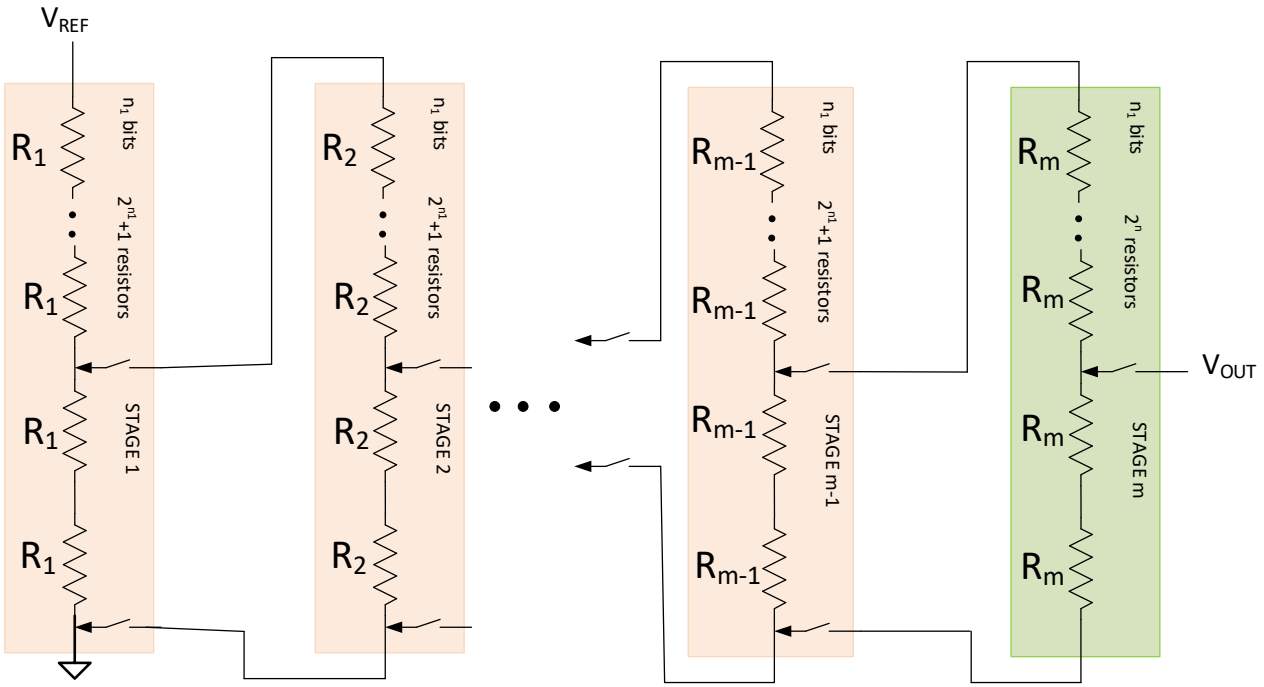


Small decoder needed to control switches

Kelvin-Varley Divider

Concept Can Be Extended to Any Base

- Shown as binary divider (n_1 bits/stage)
- $2^{n1}+1$ resistors in each string except last which has 2^{n1}



$$R_j = \frac{R_{j-1}}{2^{n_1}-1}$$

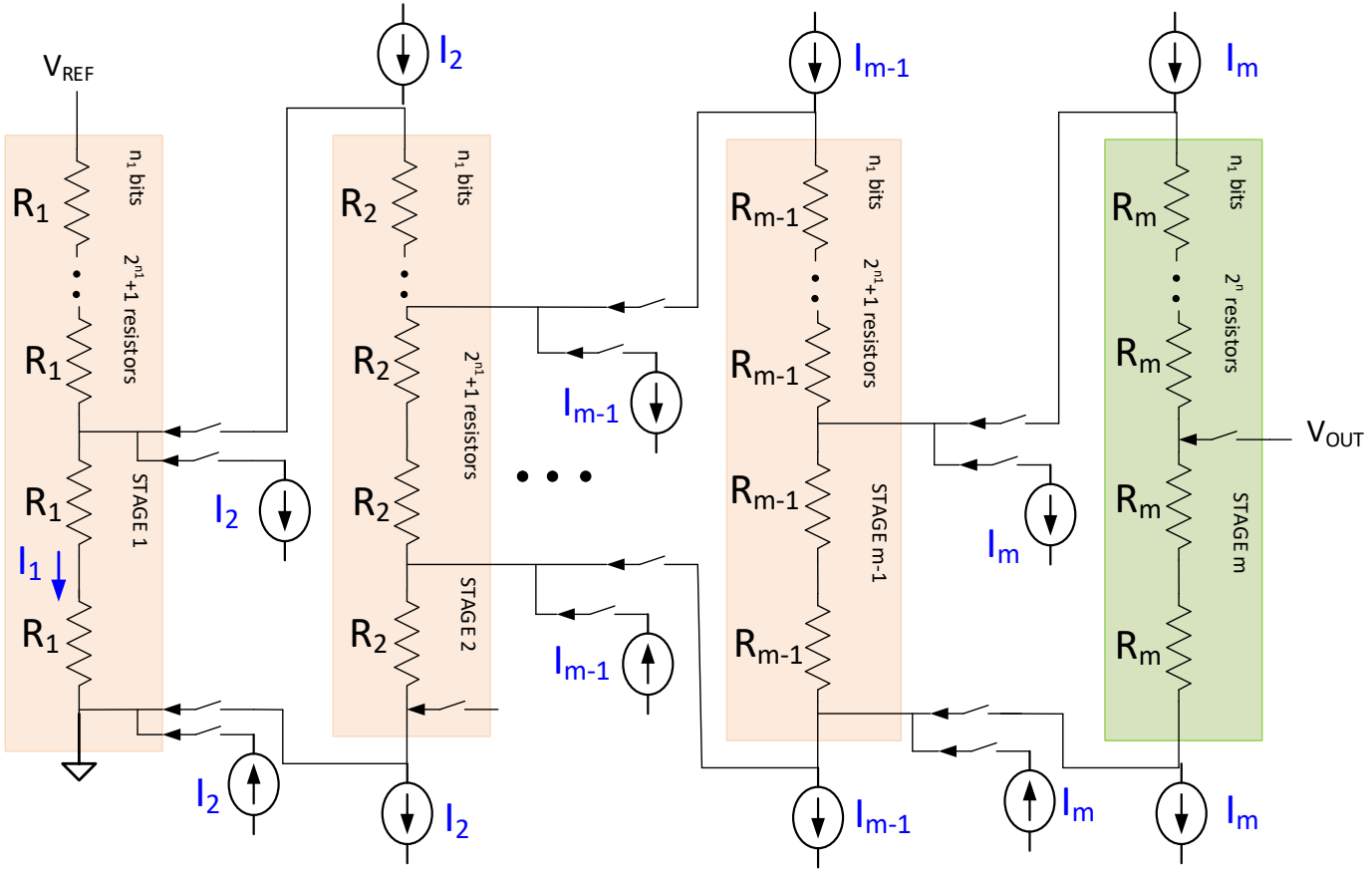
Small decoder needed to control switches

Voltage on MSB nodes ideally do not change with code

Switch impedance affects attenuation

Kelvin-Varley Divider

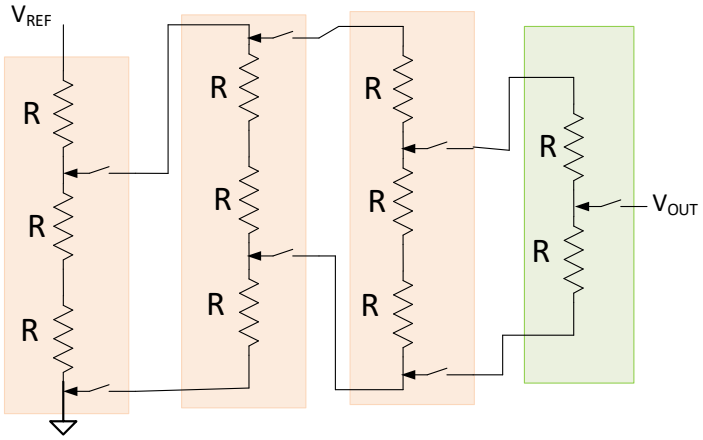
Concept Can Be Extended to Any Base



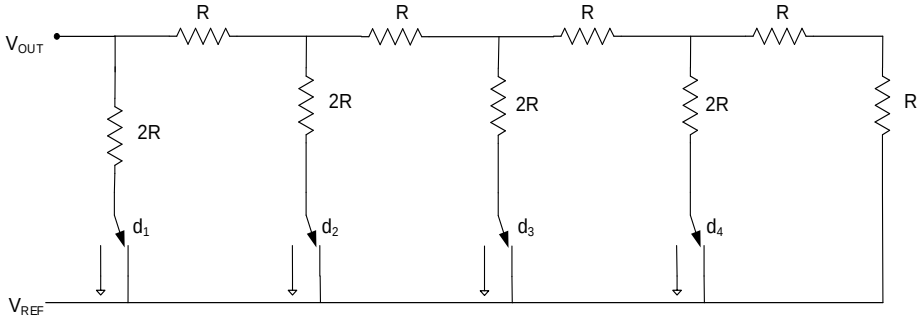
$$I_j = I_1 \qquad for\ all\ \ i$$

Switch impedance compensation

Comparison of Kelvin-Varley and R-2R



Kelvin-Varley Divider



R-2R

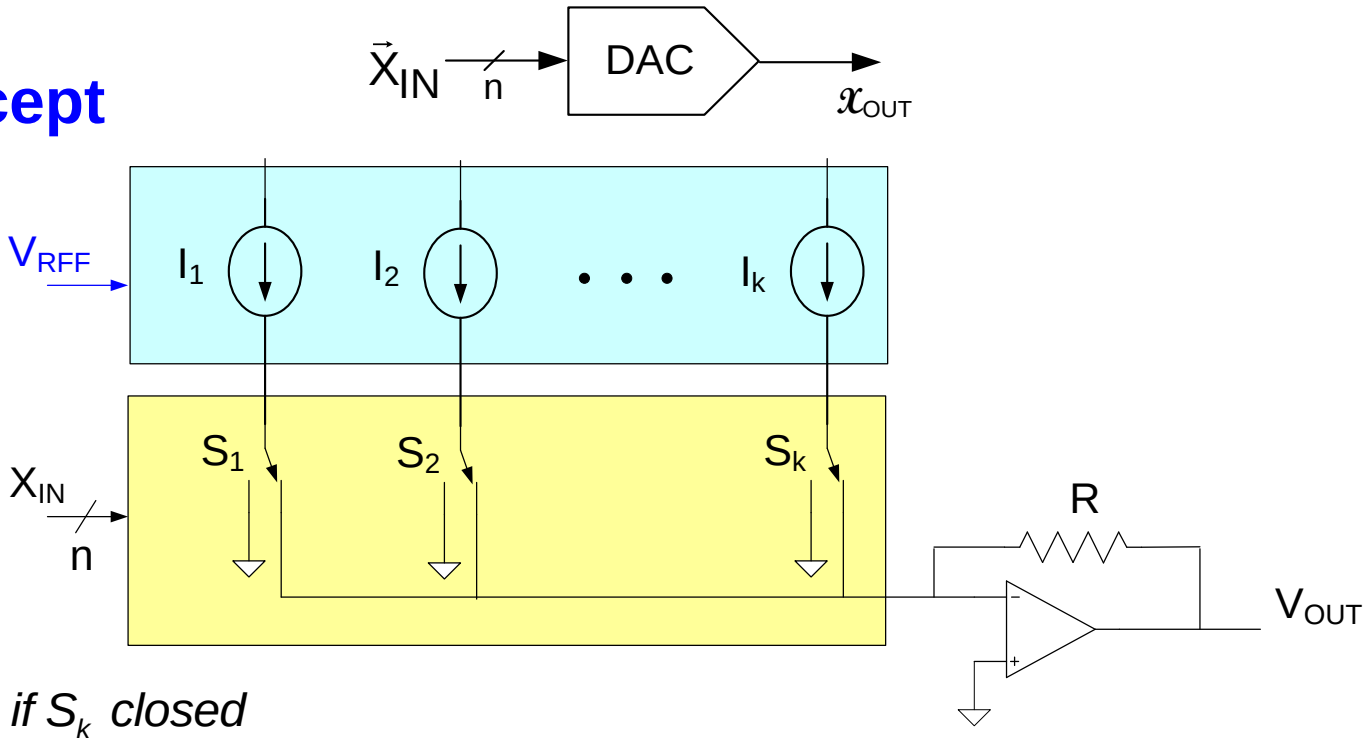
Both have 3 Resistors and 2 switches / slice

Are there any benefits of the KV structure relative to the R-2R structure?

Current Steering DACs

Current Steering DACs

Concept



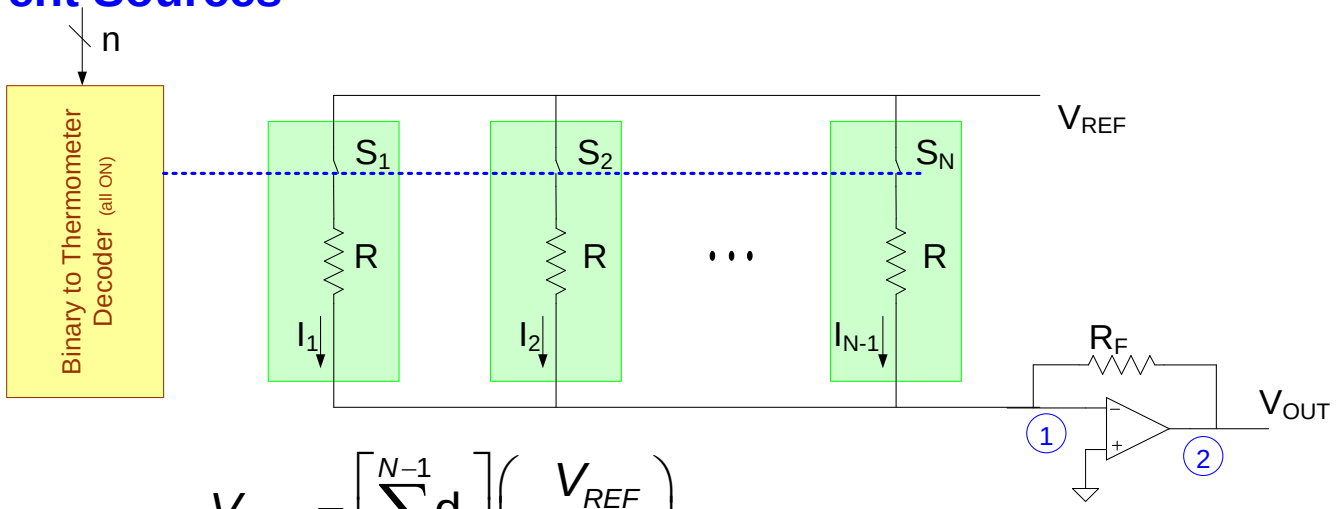
$$d_k = \begin{cases} 1 & \text{if } S_k \text{ closed} \\ 0 & \text{if } S_k \text{ open} \end{cases}$$

$$V_{OUT} = \left[\sum_{I=1}^{k} d_i I_i \right] (-R)$$

- Current sources usually unary or binary-bundled unary
- Termed bottom-plate switching
- Can eliminate resistors from DAC core
- Op Amp and resistor R can be external
- Can use all same type of switches
- Switch impedance not critical nor is switch matching
- Popular MDAC approach

Current Steering DACs

Unary Current Sources



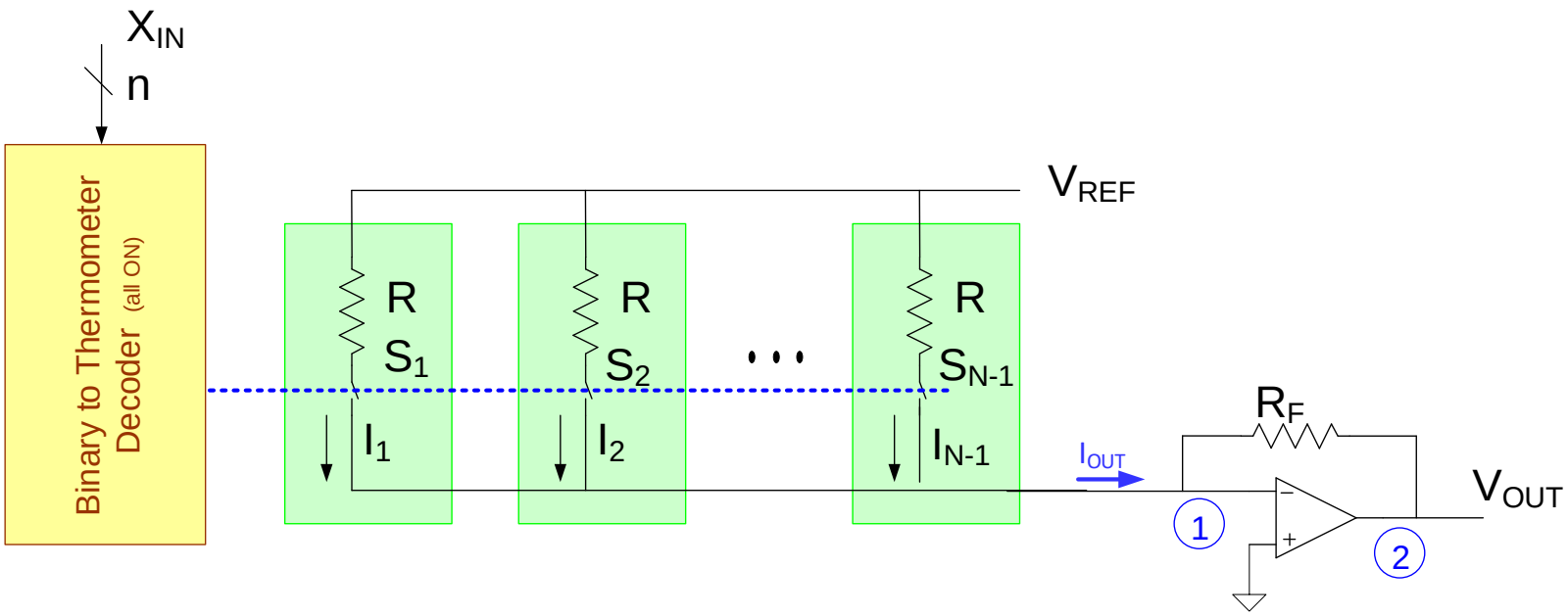
$$V_{OUT} = \left[\sum_{I=1}^{N-1} d_i\right]\left(-\frac{V_{REF}}{R}\right)$$

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed “top plate switching”
- Thermometer coding (routing challenge!)
- Excellent DNL properties
- INL may be poor, typically near mid range
- Switch kickback to V_{REF}
- Not suitable for use as MDAC

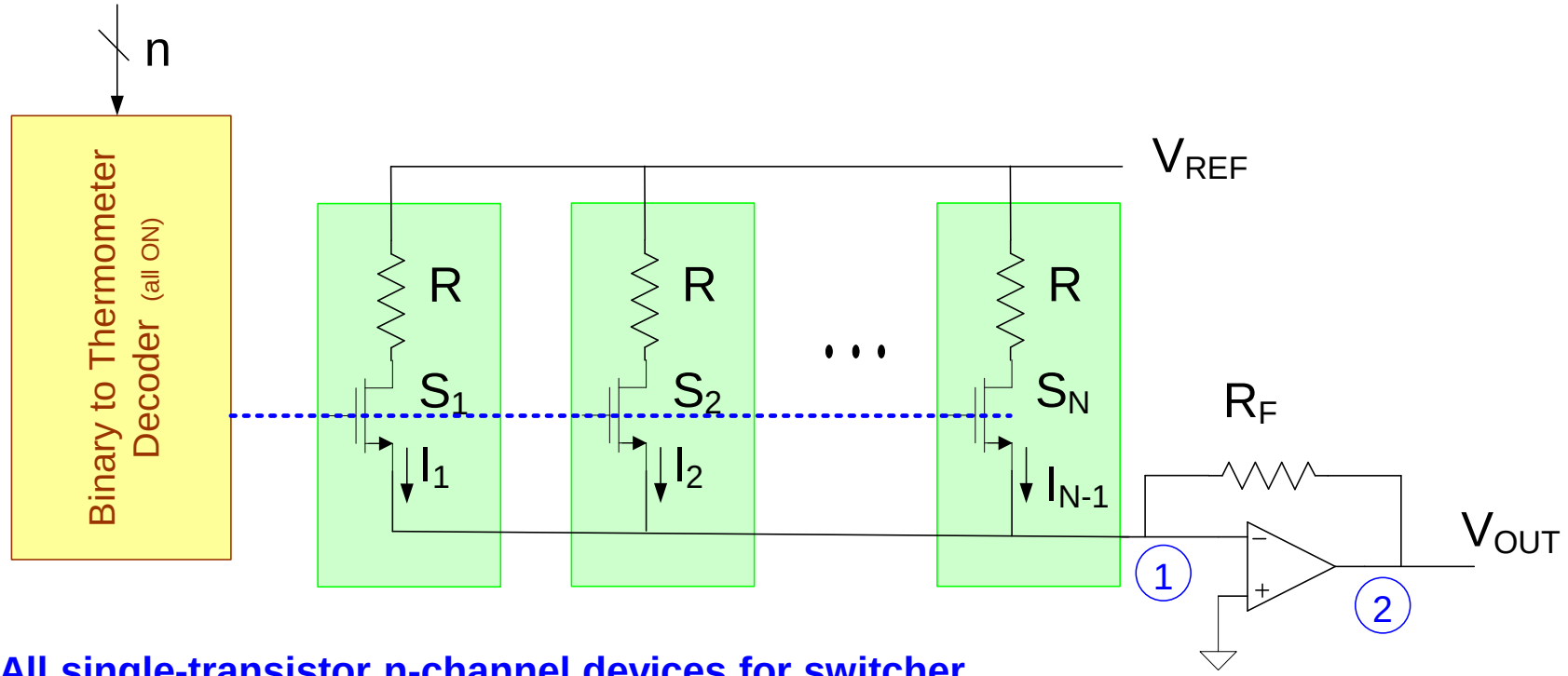
Current Steering DACs

Unary Current Sources



- **Inherently Insensitive to Nonlinearities in Switches and Resistors**
- **Smaller ON resistance and less phase-shift from clock edges**
  - Termed “bottom plate switching”
  - Thermometer coded
  - Can be used as MDAC
  - Reduced kickback to V_{REF}

Current Steering DACs



- **All single-transistor n-channel devices for switcher**
- **Unary R:switch cells**
- **Parasitic capacitances on drain nodes of switches cause transient settling delays**
- **R+Rsw is nonlinear (so nonlinear relationship between I_k and V_{REF}) but does not affect linearity of DAC**
- **Resistor and switch impedance matching important**
- **Previous code dependent transient** (parasitic capacitances on drains of switches)

Stay Safe and Stay Healthy !

End of Lecture 14